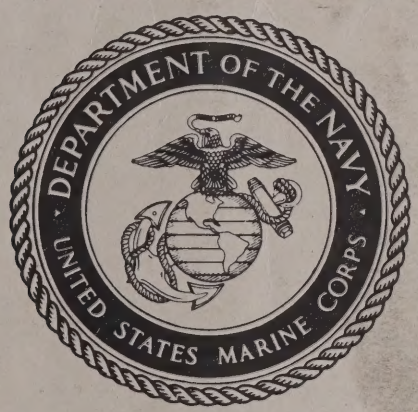
TM-08109A-13

PRELIMINARY

U.S. MARINE CORPS TECHNICAL MANUAL

OPERATION AND MAINTENANCE INSTRUCTIONS

INTERFACE UNIT TEST SET TS - 3809/TYC



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MAY 1979

RECORD OF CHANGES

CHANGE NO.	DATE	TITLE OR BRIEF DESCRIPTION	ENTERED BY

LIST OF EFFECTIVE PAGES

Insert latest changed pages; dispose of superseded pages in accordance with applicable regulations.

NOTE: On a changed page, the portions of the text affected by the latest change is indicated by a vertical line, or other change symbol, in the outer margin of the page. Changes to illustrations are indicated by miniature pointing hands. Changes to wiring diagrams are indicated by shaded areas.

Total number of pages in this manual is 146 consisting of the following:

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A - B	0	2-55	0
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LIST OF ILLUSTRATIONS

SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all times observe all safety regulations. Do not replace components inside the equipment with the line voltage turned on. To avoid casualties, always remove power and discharge and ground a circuit before touching it.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into or enter the enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation. Such information may be obtained from the Bureau of Medicine and Surgery.

The following cautions and warnings appear in the text in this volume, and are repeated here for emphasis.

To prevent damage to the equipment, set POWER to OFF before unplugging cable.
(Page 3-16).

When performing the procedure to determine cause for CHARACTER COUNT not incrementing properly in test, use care to prevent damage to equipment.
(Page 3-18).

To prevent damage to equipment, remove ac power from the AIUTE and the subsystem under test before performing replacement procedures.
(Page 3-19).

CAUTION

When removing and replacing pluggable module, align module properly to prevent bent or broken connector pins.
(Page 3-20).

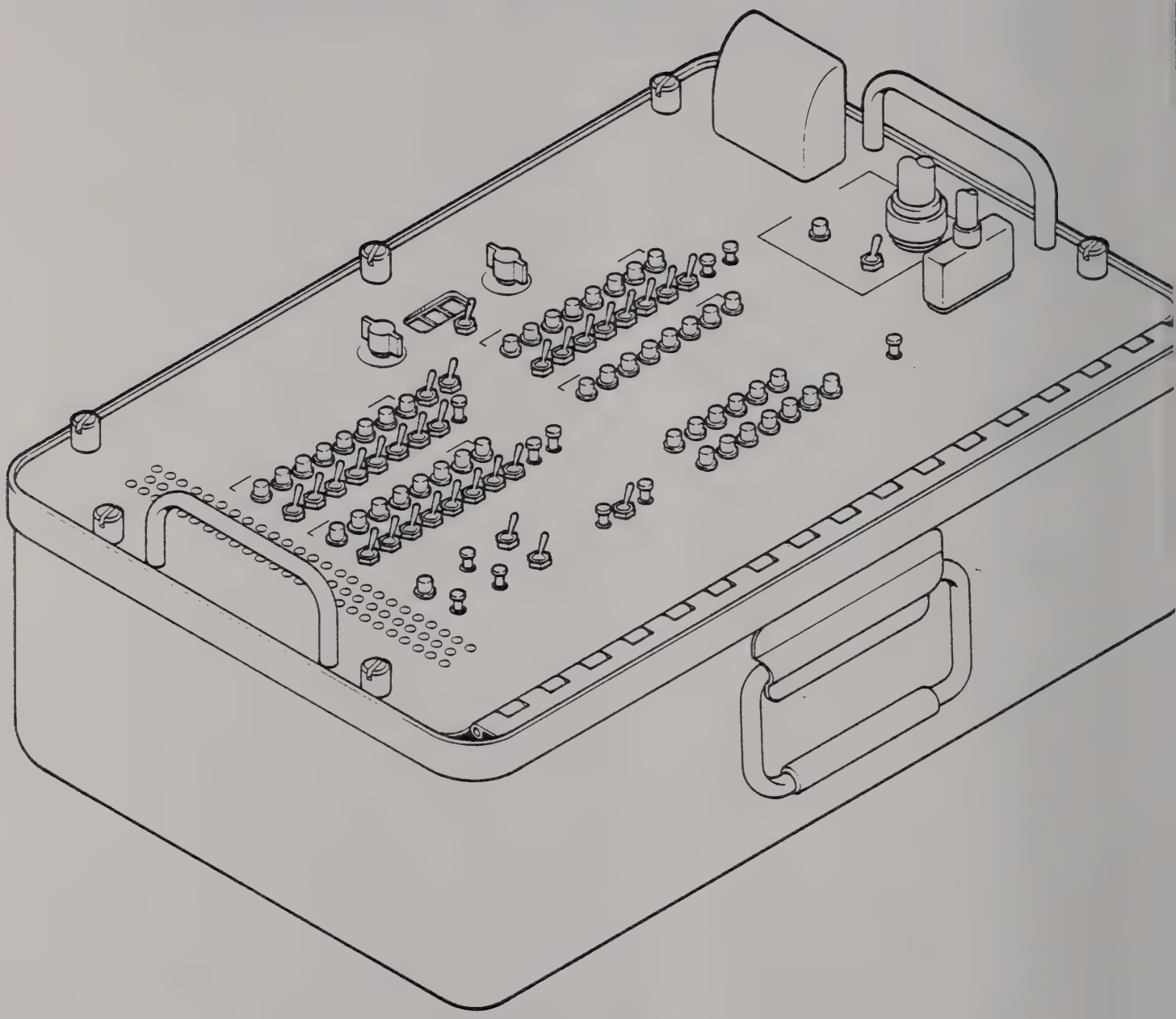


Figure 1-1. AUTODIN Interface Unit Test Equipment

CHAPTER 1

GENERAL INSTRUCTIONS

SECTION I

GENERAL DESCRIPTION AND SPECIFICATION DATA

1-1. INTRODUCTION.

1-2. SCOPE. This manual covers the operation and maintenance of the TS-3809/TYC Interface Unit Test Set. Hereafter in this manual, the Interface Unit Test Set is referred to as the AIUTE (AUTODIN Interface Unit Test Equipment). The AIUTE was procured under Contract N00104-77-A-0091, MS01, 21 February 1978.

1-3. RELATED PUBLICATIONS.

1-4. The purpose of the AIUTE is to test the AIU (AUTODIN Interface Unit) that is part of the AN/TYC-5A(V) DCT (Data Communications Terminal). The DCT Operation and Maintenance Instructions Technical Manual, TM-07115A-14, contains procedures for using the AIUTE to test the AIU.

1-5. The CP-1392/TYC Digital Electronic Counter can be used to maintain the AIUTE. The Digital Electronic Counter is documented in its own Operation and Maintenance Instructions Technical Manual, TM-XXXXX-XX.

1-6. RELATIONSHIP TO OTHER EQUIPMENT. The AIUTE requires 115 vac ±10%, 50/60 Hz, single-phase power which is available at a convenience outlet on the left side of the AIU cabinet. The AIUTE interfaces, for test, with the AIU transmitter and receiver sections.

1-7. EQUIPMENT DESCRIPTION.

1-8. Figure 1-1 shows the AIUTE with the cover of its transit case removed and with power and signal cables connected. The AIUTE consists of power and signal cable assemblies and the AIUTE wired assembly mounted in a combination transit and operating case.

1-9. PHYSICAL DESCRIPTION. Figure 1-2 shows the major assemblies of the AIUTE and table 1-1 describes characteristics of the unit.

1-10. Transit Case. The transit case consists of a main case and cover. The case includes six latches, a hinged handle, and a pressure relief valve. The cam-type latches are used to secure the cover to the main case. The hinged transport handle opens to a 90 degree stop position for carrying the AIUTE and returns to a closed position by a spring-loaded mechanism when not in use. With the cover latched, the entire case is

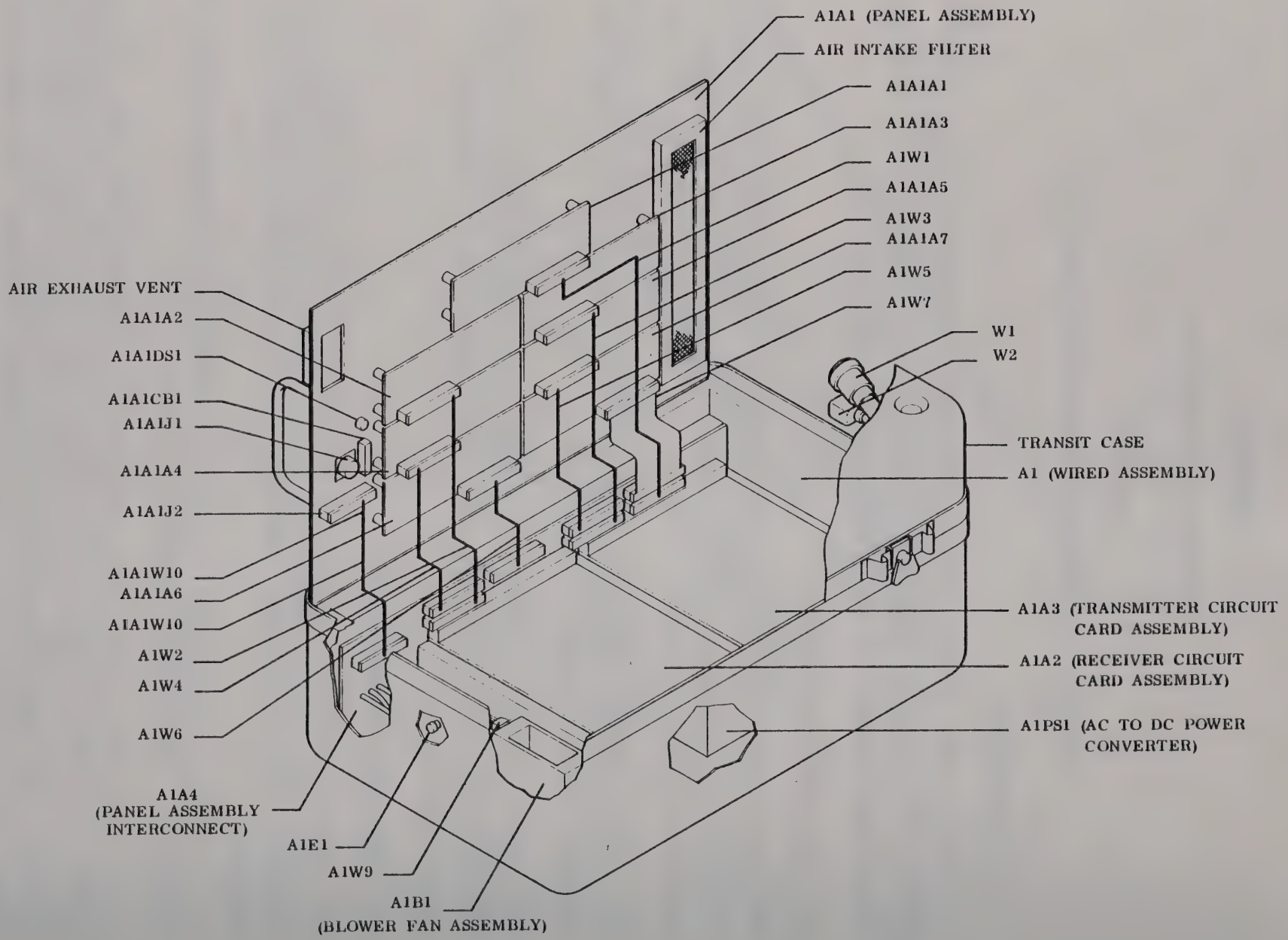


Figure 1-2. AIUTE Reference Designation Breakdown

Table 1-1. AIUTE Characteristics

CHARACTERISTIC	DESCRIPTION
Nomenclature	TS3809/TYC Interface Unit Test Set
Mission	Exercises the AN/TYC-5A(V) DCT AIU transmitter and receiver sections using applicable mode I channel coordination procedures. Operates independently in a self-test mode.
Service Conditions	
• Operating Temperature Range	0° to +50°C (32° to 122°F)
• Non-Operating Temperature Range	-55° to +71°C (-48° to +160°F)
• Operating Atmospheric Pressure Range	Sea level to 10,000 feet
• Non-Operating Atmospheric Pressure Range	Sea level to 40,000 feet
• Operating and Non-Operating Relative Humidity	Up to 95%
• Transportability	In transit case withstands loads and accelerations resulting from transport by cargo aircraft, ship, truck, rail, helicopter, and landing craft.
Message Handling	Capable of receiving and transmitting messages prepared in accordance with JANAP 128 formatting procedures.
Message Rate	Selectable; 600, 1200, 2400, or 4800 baud.
Power Requirements	115 ±10% vac, 50/60 Hz, single phase
Power Dissipation	75 watts
Dimensions	19.75 inches long by 13.87 inches wide by 10.00 inches high
Weight	35 pounds
Cooling	Self-contained blower fan

atmospherically sealed except for the automatic pressure relief valve. The interior of the case cover contains a hinged drop leaf panel with quick-operating fasteners. A storage area for the cable assemblies, panel brace, and this manual is located under this panel.

1-11. Wired Assembly, A1. The AIUTE wired assembly consists of a chassis enclosure with a hinged operator's panel assembly on top. The interior of the chassis houses the receive and transmit tester circuit card assemblies, panel assembly interconnect, power converter, and blower fan. Interconnections for cables A1W1 through A1W7 and A1W9 are shown in figure 2-7.

1-12. Panel Assembly, A1A1. The panel assembly is hinged to the bottom of the chassis and secured by captive screws. When the captive screws are loosened, the panel can be raised to a vertical position by using the two panel protector/handles. This provides maintenance access to back panel assemblies and assemblies mounted within the chassis. A panel brace, stored in the transit case cover, can be mounted on the inside of the raised panel and on the chassis mounting flange to secure the panel during maintenance. The panel contains seven switch-indicator assemblies (A1A1A1 through A1A1A7). Figure 1-3 shows a typical switch-indicator assembly. Each assembly consists of a printed wiring board with switch-indicator components and a 40-pin connector. The panel also contains the power interface connector (A1A1J1), 25-pin signal interface connector (A1A1J2), power circuit breaker (A1A1CB1), power indicator (A1A1DS1), air intake filter, and air exhaust vent. Interconnections for cable A1A1W1 through A1A1W7 and A1A1W10 are shown in figure 2-7.

1-13. Receiver and Transmitter Circuit Card Assemblies, A1A2 and A1A3. The receiver circuit card assembly (A1A2) and the transmitter circuit card assembly (A1A3) are located inside the chassis. Figure 1-4 shows a typical circuit card assembly. These cards each consist of a multilayer printed wiring board with components (integrated circuits, capacitors, and resistors) mounted on the top surface and a connector mounted on one end. The cards plug into two 159-pin connectors on the panel assembly interconnect board.

1-14. Panel Assembly Interconnect, A1A4. The panel assembly interconnect is located inside the chassis. The assembly, shown in figure 1-5, consists of a power and ground plane printed wiring board with components mounted on each side. The power and ground planes distribute +5 vdc power and ground to the board components. One side of the board contains seven 40-pin connectors (A1A4J2 through A1A4J5, A1A4J7, A1A4J9, and A1A4J10), one 25-pin connector (A1A4J6), and two 159-pin connectors (XA1A2 and XA1A3). The 40-pin connectors interface with the panel switch-indicator assemblies. The 25-pin connector interfaces with the panel signal interface connector. The 159-pin connector receptacles mate with connectors on the receiver and transmitter circuit card assemblies. This side of the board also contains terminals A1A4E1 through A1A4E10. Terminals A1A4E3 through A1A4E6 interface the power and ground plane with the ac to dc power converter A1PS1. The other side of the board contains four capacitors (A1A4C1 through A1A4C4), a dc to dc power converter (A1A4PS1), and the connector wrap posts. The dc to dc power converter receives input power from the power and

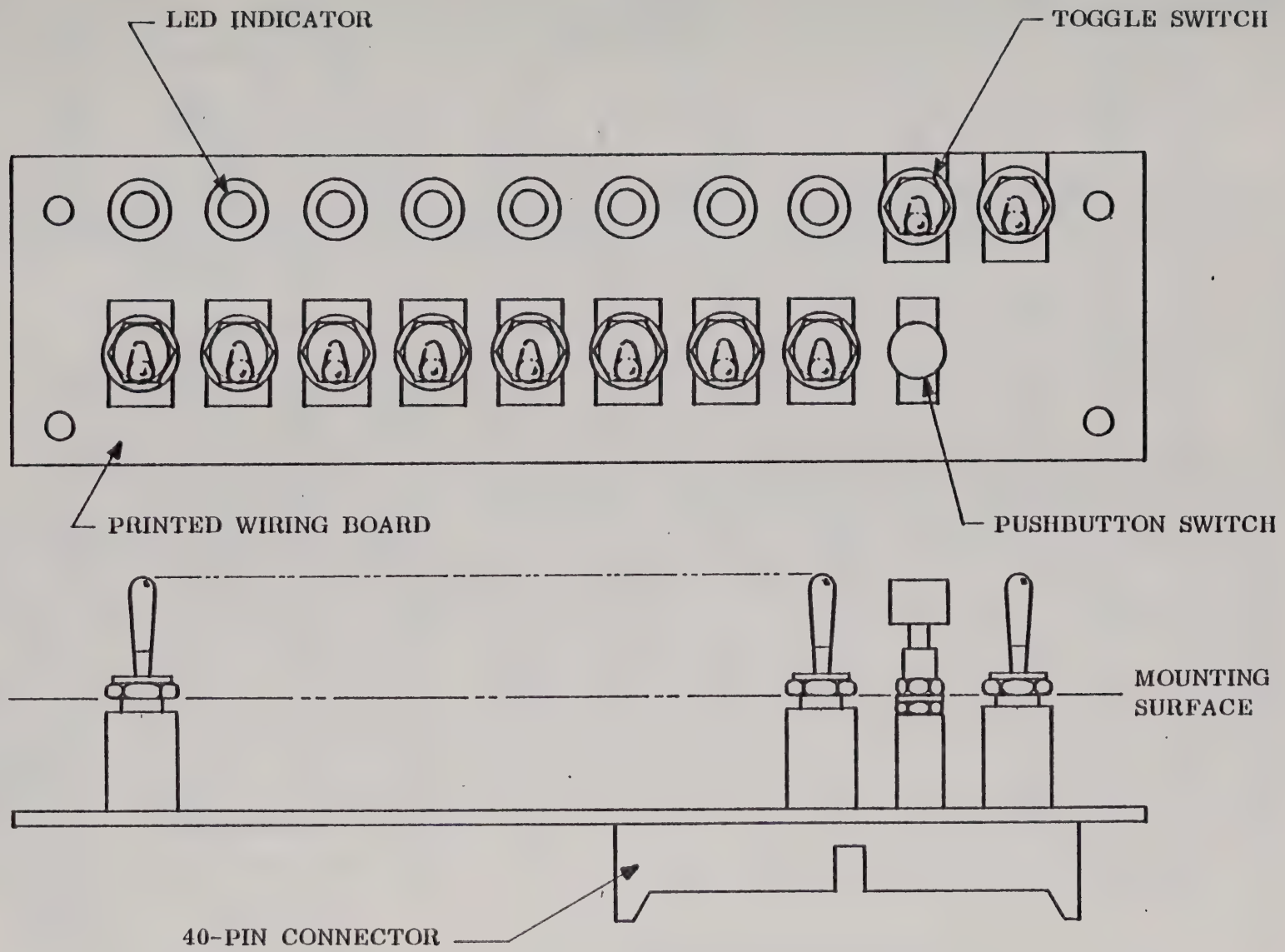


Figure 1-3. Typical Switch-Indicator Assembly

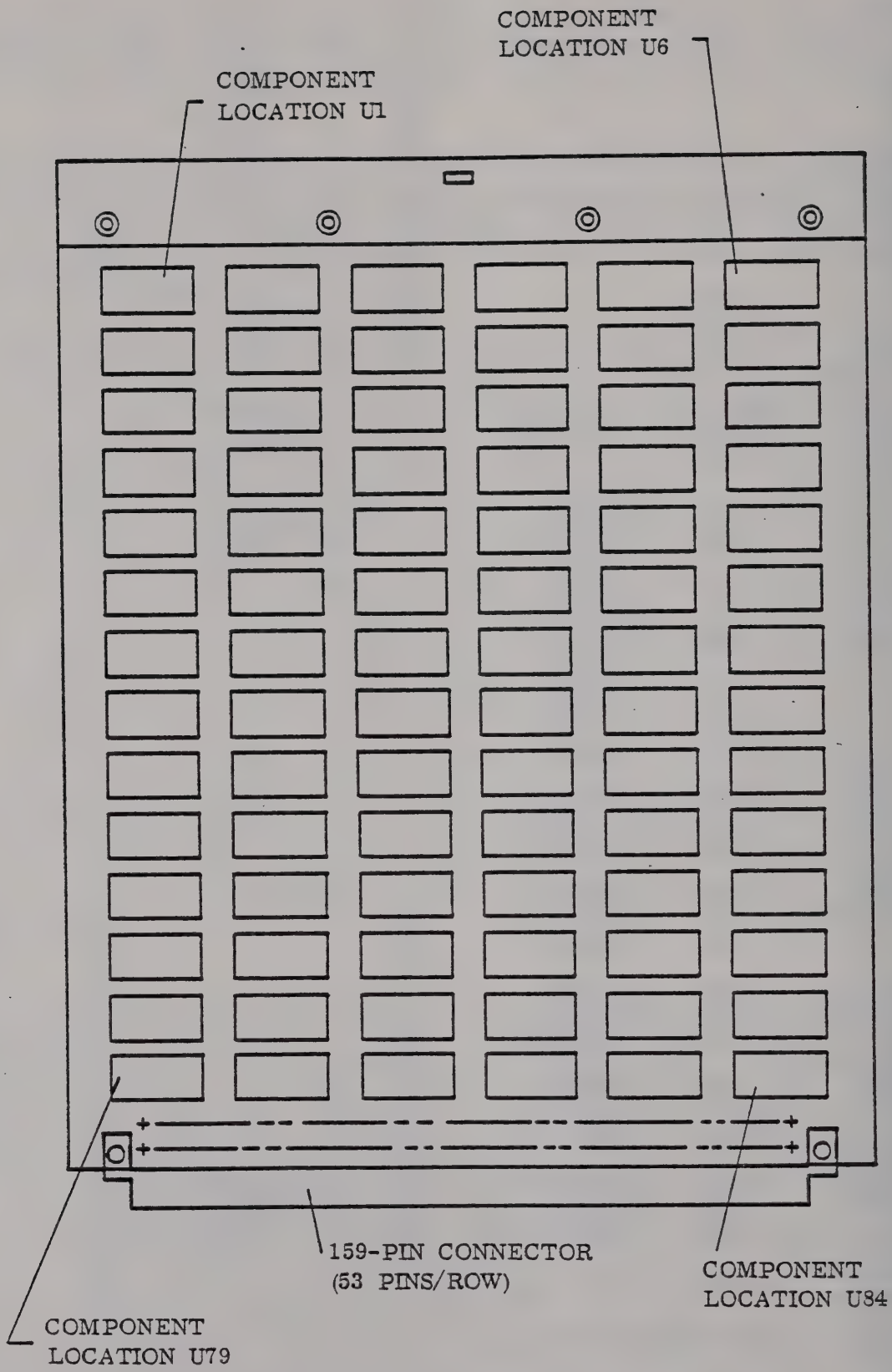


Figure 1-4. Circuit Card Assembly

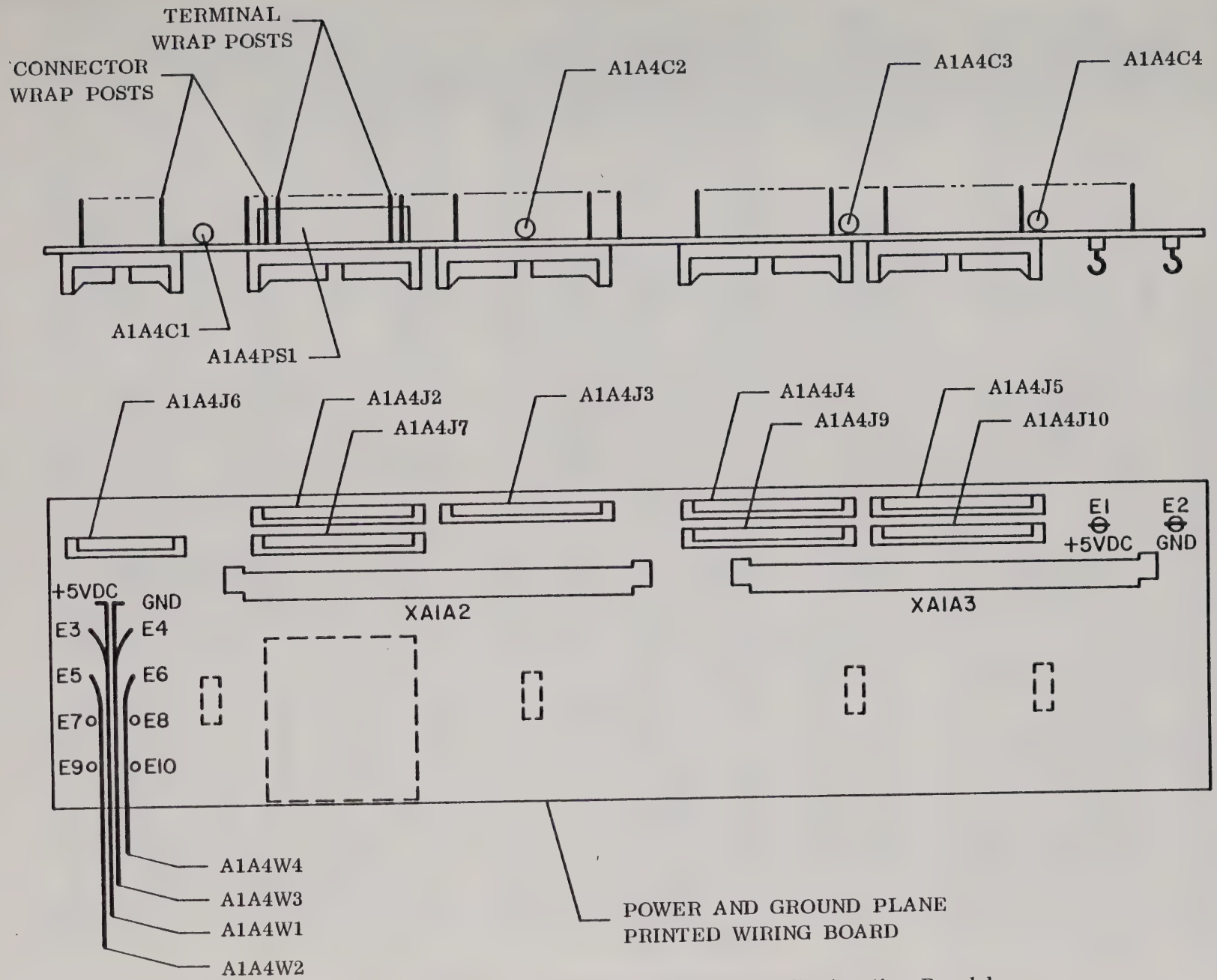


Figure 1-5. Panel Assembly Interconnect Reference Designation Breakdown

ground planes, and provides ±12 vdc output power to terminal wrap posts. The connector and terminal wrap posts are wire-wrapped on this side of the board. Interconnections for cables A1A4W1 through A1A4W4 are shown in figure 2-7.

1-15. Ac to Dc Power Converter, A1PS1. The ac to dc power converter is mounted inside the chassis under the receiver and transmitter circuit card assemblies. The supply receives 115 vac ±10%, 50 or 60 Hz, single-phase power and provides a nominal 5 vdc output to the chassis. The output is adjustable by a screwdriver adjustable potentiometer located at one end of the supply. The opposite end of the supply contains a terminal board to interconnect ac power with the panel circuit breaker, blower fan, and power input connector. Dc power is distributed from this terminal board to the power-ground plane on the panel assembly interconnect board.

1-16. Blower Fan, A1B1. The blower fan is located inside the chassis, on the right side (as viewed from the normal operating position with the panel down), and draws cooling air through the panel air intake filter, over the assemblies, and out an exhaust vent on the panel. The blower is interconnected with input power by the terminal board on the ac to dc power converter.

1-17. FUNCTIONAL DESCRIPTION. Figure 1-6 shows a block diagram of the AIUTE. Bit serial and character serial data is transferred between the AIUTE and AIU. The transfer of each bit is controlled by the Tx and Rx clock from the AIUTE. The data transfers consist of data characters, framing characters, or control characters. The AIUTE receiver section simulates a remote terminal to exercise the AIU transmitter for test. The AIUTE transmitter section simulates a remote terminal to exercise the AIU receiver for test. Prior to an exchange of data, the AIUTE and the AIU must be synchronized. When the AIU and AIUTE are powered up and master cleared, the two units transmit SYN characters continuously to enter character synchronization. When the CANCEL switch on the AIU and the CAN switch on the AIUTE are pressed, the two units exchange CAN and ACK 2 characters to complete character synchronization.

1-18. Receiver Section. The receiver section exercises the AIU transmitter for test. After character synchronization has been established, the AIU continues to send SYN characters to maintain character synchronization. The appropriate input subsystem is made ready to send a one, two, or three-block message. The AIU transmits each bit of the message on each occurrence of the Tx clock from AIUTE. The AIUTE receiver assembles each bit received into an 8-bit shift register. When one character has been received, it is stored in a holding register and examined by the receiver logic. If the character is the first framing character of a block (SOH or STX), it is written in the RAM, and the RAM address register increments for the next character. If the character is a control character, it is not written in the RAM, but is processed separately and lights an indicator on the AIUTE panel. The AIU continues to send the message characters: the second framing character (select or DEL), 80 text characters, the third framing character (ETB or ETX), and the fourth framing character (block parity). The AIUTE receiver stores each character in the RAM and checks the fourth framing character for correct block parity. If a parity or other error is detected, the receiver sends a NACK request to the AIUTE transmitter. The AIUTE transmitter then sends a

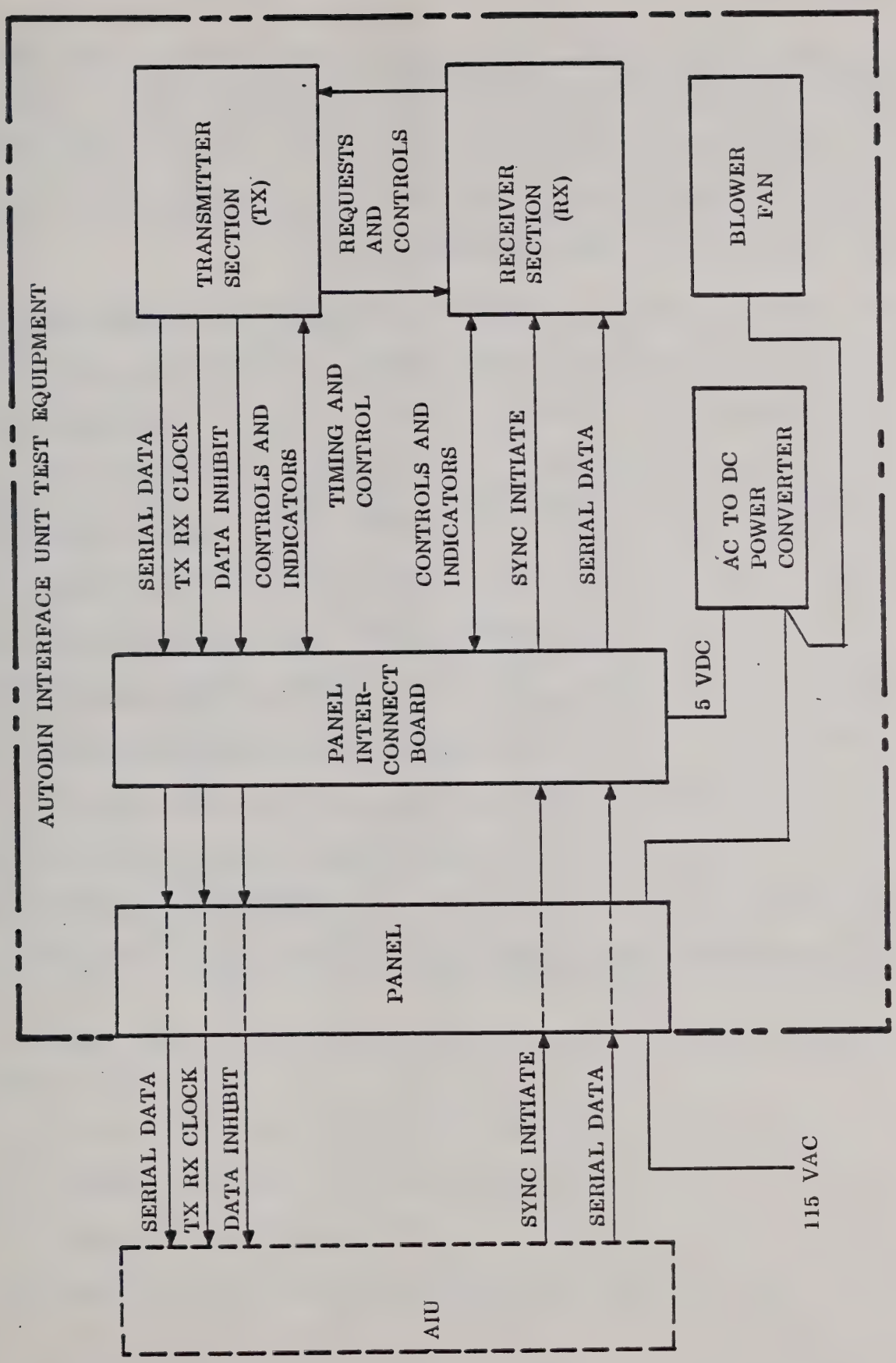


Figure 1-6. AIUTE Block Diagram

NAK control character sequence to the AIU, and the AIU transmits the block again. For a message block properly received, the AIUTE receiver sends an ACK 1 or ACK 2 request to the AIUTE transmitter. The AIUTE transmitter then sends an ACK 1 or ACK 2 control character sequence to the AIU. The ACK 1 and ACK 2 control characters are sent alternately for each block received properly. The ACK 1 is returned after the first block of a message. When a message has been transmitted and written in the RAM, the memory can be examined by the operator on the AIUTE panel indicators to determine if the AIU properly transmitted the message.

1-19. Transmitter Section. The transmitter section exercises the AIU receiver for test. After character synchronization has been established, the AIUTE transmitter continues to send SYN characters to maintain character synchronization. The appropriate output subsystem is made ready to receive a one, two, or three-block message. The AIUTE transmitter reads an eight-bit character from the ROM (read-only memory) or RAM (read/write memory) when the START switch is pressed. The ROM or RAM is selected by a switch on the panel. The ROM contains a three-block message loaded by the manufacturer at the factory. The RAM, if selected, must first be loaded by the operator with a one, two, or three-block message. In either case, an even parity select character must be written in the RAM by the operator before a message can be transmitted. When the START switch is pressed, the first framing character is read from memory and loaded into the serial output register. The memory address register is incremented to read the next character. Each bit of the first framing character is transmitted to the AIU and the second framing character read from memory is loaded into the serial output register. When the second framing character has been transferred to the AIU, the transmitter section increments the address register or, if a control character signal is received from the receiver section, addresses the control character ROM. The first text character or a control character is then transmitted to the AIU. When the text characters and the third framing character of a block have been transmitted, the transmitter generates the fourth framing character and transmits it to the AIU. The transmitter starts its answer timer and, if the proper response to the block transfer is not received from the AIU at the receiver, the transmitter addresses the control character ROM for a REP character, and transmits the REP control character sequence. When a one, two, or three-block message has been transferred, the selected DCT output subsystem medium (paper tape, punched cards, magnetic tape) can be examined to see if the AIU properly received the right message.

CHAPTER 1

SECTION II

PREPARATION FOR USE

1-20. GENERAL.

1-21. This section contains unpacking and preparation procedures for the AIUTE.

1-22. UNPACKING.

1-23. The AIUTE is contained in a combination transit and operating case, and for shipment it is packaged in a corrugated cardboard container. Unpack the AIUTE from the container as follows:

a. Cut and remove reinforced tape seal.

b. Open container and remove density foam padding.

c. Open polyethylene film moisture/dust barrier.

d. Grasp and open hinged handle of transit case.

e. Lift transit case clear of packaging material.

f. Transport to shelter or storage area.

1-24. PREPARATION FOR USE.

1-25. The location of the AIUTE in the test setup is optional within cable length of the AIU cabinet.

1-26. TEST SETUP. To prepare the AIUTE for use and to configure the test setup, proceed as follows:

a. Remove AIUTE from shelter test equipment storage area.

b. Transport and locate AIUTE near AIU cabinet.

c. Unlatch six cover latches on transit case.

d. Remove cover from main case and place clear of test area.

e. Locate hinged panel inside case cover.

f. Unlatch panel fasteners and open panel using finger hole.

g. Remove power cable assembly W1.

h. Remove signal cable assembly W2, then latch panel.

i. Install power cable at connector J1 on tester panel.

j. Install signal cable at connector J2 on tester panel.

k. Power-down the AIU. (Refer to Chapter 1, Section II of DCT Operation and Maintenance Instructions Manual, TM-07115A-14.)

l. Loosen captive screws on AIU front panel.

m. Grasp AIU panel handles and slide fully forward.

n. Locate AIU electronic chassis assembly A4A2 (in upper right corner of AIU).

o. Loosen captive screws and slide electronic chassis assembly forward out of its brackets. Set assembly on top of wired connector assembly A2.

p. On electronic chassis assembly, remove cable connector at location A16.

q. Plug module type cable connector of AIUTE signal cable W2 into location A16.

1-27. POWER-UP AND INITIAL CHECKOUT. The following paragraphs contain procedures to power-up and check out the AIUTE.

1-28. AIUTE Power-Up. To power-up the AIUTE, proceed as follows:

a. Plug power cable W1 into convenience outlet on AIU cabinet.

b. Set POWER switch to ON.

c. Observe that POWER indicator lights and that blower fan is operating.

1-29. AIUTE Checkout. To check out the AIUTE, power-up the AIUTE and proceed as follows:

a. Configure panel switches as follows:

1. Set SELF TEST switch up.

2. Set all TRANSMIT ADDRESS switches down.

3. Set all TRANSMIT DATA switches down.

4. Set TRANSMIT CONTROL/BP ERROR switch down.

5. Set TRANSMIT CONTROL/DATA INH switch down.

6. Set all RECEIVE ADDRESS switches down.

7. Set MSG Y/R switch to R.

8. Set MEM RAM/ROM switch to ROM.

9. Position CLOCK SELECT switch to 600.

10. Position MODE SELECT switch to BLK.

b. Press MC switch and observe following:

1. TRANSMIT DATA indicators 8, 5, 3, and 2 light.

2. RECEIVE DATA indicators 8, 5, 3, and 2 light.

3. RECEIVE CONTROL/SYNC indicator lights.

4. RECEIVE CONTROL/RM indicator lights.

5. CHARACTER COUNT = 000.

c. Press TRANSMIT CONTROL/CAN switch and observe following:

1. RECEIVE CONTROL/RM indicator goes off.

2. RECEIVE CONTROL/ACK 2 indicator lights.

d. Set SELF TEST switch down.

1-30. PREPARATION FOR RELOCATION.

1-31. POWER-DOWN AND DISCONNECT. To power-down and disconnect the test setup, proceed as follows:

a. Power-down the AIU. (Refer to Chapter 1, Section II, of DCT Operation and Maintenance Instructions Manual, TM-07115A-14.)

b. Set AIUTE POWER switch to OFF.

c. Unplug AIUTE power cable W1 at AIU cabinet convenience outlet.

d. On AIU electronic chassis assembly, location A16, remove module type cable connector of AIUTE signal cable W2.

e. Reinstall AIU electronic chassis assembly cable connector at location A16.

f. Reinstall AIU electronic chassis assembly and tighten captive screws.

g. Slide AIU panel back into place and tighten captive screws.

1-32. RELOCATION. To relocate the AIUTE, proceed as follows:

a. Locate panel inside transit case cover.

b. Unlatch panel fasteners and open panel.

c. Store power cable assembly W1 inside cover.

d. Store signal cable assembly W2 inside cover.

e. Close panel and latch fasteners.

f. Mount transit case cover on main case and secure cover with transit case latches.

1-33. PREPARATION FOR LIMITED STORAGE AND RESHIPMENT. There are no limited storage preparation requirements for the AIUTE when stored in the shelter support equipment storage area, or a separate storage van, other than having the cover fully latched to the main case. For reshipment of the AIUTE or any of its assemblies, proceed as follows:

a. Wrap in polyethylene film moisture/dust barrier.

b. Place in corrugated cardboard container (rated at 200 pounds per square inch bursting strength or more).

c. Surround on all sides by 2-inch, 1.5-pound density foam padding.

d. Seal container with reinforced tape.

CHAPTER 1

SECTION III

DEMOLITION TO PREVENT ENEMY USE

1-34. GENERAL.

1-35. When capture or abandonment of the AIUTE to an enemy is imminent, the responsible unit commander must make the decision to either destroy or render the equipment inoperable. Based on his decision, orders are issued which cover the desired extent of destruction.

1-36. DEMOLITION TO RENDER AIUTE INOPERATIVE.

1-37. When orders are issued to render the AIUTE inoperative, thermite grenades, sledge hammers, pickaxes, or other tools that are available can be used to demolish the unit.

CHAPTER 2

OPERATING INSTRUCTIONS

SECTION I

THEORY OF OPERATION

2-1. INTRODUCTION.

2-2. SCOPE. This section contains a description of the test message format and provides general and detailed descriptions of the AIUTE. The AIUTE was designed for configuration in a test setup within the shelter to support troubleshooting procedures for the DCT AIU.

2-3. SIGNAL LEVELS. The signal levels for the AIUTE are as follows:

a. Internal: true = +3.5 volts; false = +0.5 volts.

b. Interface: true = +6.0 volts; false = -6.0 volts.

2-4. MESSAGE DESCRIPTION.

2-5. MESSAGE STORAGE. The receiver and transmitter sections of the AIUTE each contain a 256 by 8-bit RAM. In addition, the transmitter contains a 512 by 8-bit ROM. The receiver RAM is loaded during AIU testing with a one, two, or three block message received from the AIU. The transmitter RAM is loaded with a one, two, or three block message by operator action at the AIUTE panel. A three-block message consists of 252 8-bit characters. The receiver RAM has a wraparound capability so that a received message in excess of three blocks is stored as follows: block 4 is stored over (and destroys) block 1, block 5 is stored over (and destroys) block 2, and so forth. The transmitter ROM is loaded with two three-block messages by the manufacturer at the factory. This message cannot be changed. Since the select character is variable, depending on the output peripheral subsystem used, the desired select character must be loaded by the operator into the transmitter RAM before test using the ROM. The AIUTE automatically addresses the transmitter RAM for the select character. The select characters are as specified below:

Select Character	Medium	Bits							
		8	7	6	5	4	3	2	1
A	Paper tape, ITA-2 format (5-level).	0	1	0	0	0	0	0	1
H	Paper tape, ASCII format (8-level).	0	1	0	0	1	0	0	0
S	Flash S (high priority paper tape).	0	1	0	1	0	0	1	1
D	Punched card.	0	1	0	0	0	1	0	0
F	Flash F (high priority punched card).	1	1	0	0	0	1	1	0
*E	Magnetic tape.	1	1	0	0	0	1	0	1
*C	Magnetic tape.	1	1	0	0	0	0	1	1

*Variable depending on controller capability.

2-6. MESSAGE FORMAT. The message format consists of ASCII (American Standard Code for Information Interchange) characters. Each character consists of seven data bits and one parity bit. Each block of the message consists of four framing characters and 80 text characters. The first framing character is the even parity SOH (start of header) or STX (start of text) character. The second framing character is the even parity select or DEL (delete) character. The first two framing characters are followed by 80 odd parity text characters. The third framing character is the even parity ETB (end of transmission block) or ETX (end of text) character. The fourth framing character is the BP (block parity) character, which is either even or odd parity. The ROM contains two three-block messages, one formatted in GENSER (R) and one formatted in DSSCS (Y). Selection of the R or Y format is made by the MSG switch on the panel.

2-7. Message Content. The content of the RAM text characters in a message is determined by the user. The content of the transmitter ROM is defined in table 2-1.

2-8. MESSAGE CONTROL CHARACTERS. The message control characters consist of ASCII characters. Each character consists of seven data bits and one parity bit. The message control characters include receive control characters (ACK 1, ACK 2, NAK, RM, or WBT), transmit control characters (REP or CAN), and special control characters (EM or SYN). The receive control characters are sent as an identical, adjoining pair (sequence). These characters are sent as an answer to a received block or as a response to transmit control characters. The receive control characters are ACK (acknowledge) 1, ACK 2, NACK (negative acknowledge), RM (reject your message), and WBT (wait before transmitting). They can be sent anytime except between two adjacent framing characters. The transmit control characters are also sent as an identical,

Table 2-1. Contents of AIUTE Transmitter ROM

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
SOH	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
(Select)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0
C	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1
C	0	1	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0
U	1	1	0	1	0	1	0	1	0	0	0	0	0	0	1	0	1
Z	1	1	0	1	1	0	1	0	0	0	0	0	0	0	1	1	0
Y	1	1	0	1	1	0	0	1	0	0	0	0	0	0	1	1	1
U	1	1	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0
W	0	1	0	1	0	1	1	1	0	0	0	0	0	1	0	0	1
SP	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R	0	1	0	1	0	0	1	0	0	0	0	0	0	1	0	1	1
U	1	1	0	1	0	1	0	1	0	0	0	0	0	1	1	0	0
E	0	1	0	0	0	1	0	1	0	0	0	0	0	1	1	0	1
B	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0
C	0	1	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1
D	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
C	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	1
0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1	0
0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1	1
2	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1	0	0
1	0	0	1	1	0	0	0	1	0	0	0	0	1	0	1	0	1
SP	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0
2	0	0	1	1	0	0	1	0	0	0	0	0	1	0	1	1	1
7	0	0	1	1	0	1	1	1	0	0	0	0	1	1	0	0	0
3	1	0	1	1	0	0	1	1	0	0	0	0	1	1	0	0	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA BINARY BITS								ADDRESS BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
1	0	0	1	1	0	0	0	1	0	0	0	0	1	1	0	1	0
8	0	0	1	1	0	0	0	1	0	0	0	0	1	1	0	1	0
3	1	0	1	1	0	0	1	1	0	0	0	0	1	1	1	0	0
3	1	0	1	1	0	0	1	1	0	0	0	0	1	1	1	0	1
-	1	0	1	0	1	1	0	1	0	0	0	0	1	1	1	1	0
U	1	1	0	1	0	1	0	1	0	0	0	0	1	1	1	1	1
U	1	1	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0
U	1	1	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
U	1	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0
-	1	0	1	0	1	1	0	1	0	0	0	1	0	0	0	1	1
-	1	0	1	0	1	1	0	1	0	0	0	1	0	0	1	0	0
R	0	1	0	1	0	0	1	0	0	0	0	1	0	0	1	0	1
U	1	1	0	1	0	1	0	1	0	0	0	1	0	0	1	1	0
E	0	1	0	0	0	1	0	1	0	0	0	1	0	0	1	1	1
B	1	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0
A	1	1	0	0	0	0	0	1	0	0	0	1	0	1	0	0	1
B	1	1	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0
A	1	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	1
.	1	0	1	0	1	1	1	0	0	0	0	1	0	1	1	0	0
SP	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	0	1
	S a m e								T h r u								
SP	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1
(	1	0	1	0	1	0	0	0	0	0	0	1	1	0	1	0	0
T	0	1	0	1	0	1	0	0	0	0	0	1	1	0	1	0	1
H	1	1	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
I	0	1	0	0	1	0	0	1	0	0	0	1	1	0	1	1	1
S	1	1	0	1	0	0	1	1	0	0	0	1	1	1	0	0	0
SP	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	1
I	0	1	0	0	1	0	0	1	0	0	0	1	1	1	0	1	0
S	1	1	0	1	0	0	1	1	0	0	0	1	1	1	0	1	1
SP	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0
A	1	1	0	0	0	0	0	1	0	0	0	1	1	1	1	0	1
SP	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0
T	0	1	0	1	0	1	0	0	0	0	0	1	1	1	1	1	1
E	0	1	0	0	0	1	0	1	0	0	1	0	0	0	0	0	0
S	1	1	0	1	0	0	1	1	0	0	1	0	0	0	0	0	1
T	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0
SP	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1
M	1	1	0	0	1	1	0	1	0	0	1	0	0	0	1	0	0
E	0	1	0	0	0	1	0	1	0	0	1	0	0	0	1	0	1
S	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	0
S	1	1	0	1	0	0	1	1	0	0	1	0	0	0	1	1	1
A	1	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0
G	1	1	0	0	0	1	1	1	0	0	1	0	0	1	0	0	1
E	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	1	0
)	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	1	1
SP	0	0	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0
	S a m e								T h r u								
SP	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	1
ETB	0	0	0	1	0	1	1	1	0	0	1	0	1	0	0	1	0
(BP)	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
STX	1	0	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0
DEL	1	1	1	1	1	1	1	1	0	0	1	0	1	0	1	0	1
A	1	1	0	0	0	0	0	1	0	0	1	0	1	0	1	1	0
B	1	1	0	0	0	0	1	0	0	0	1	0	1	0	1	1	1
C	0	1	0	0	0	0	1	1	0	0	1	0	1	1	0	0	0
D	1	1	0	0	0	1	0	0	0	0	1	0	1	0	0	0	1
E	0	1	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0
F	0	1	0	0	0	1	1	0	0	0	1	0	1	1	0	1	1
G	1	1	0	0	0	1	1	1	0	0	1	0	1	1	1	0	0
H	1	1	0	0	1	0	0	0	0	0	1	0	1	1	1	0	1
I	0	1	0	0	1	0	0	1	0	0	1	0	1	1	1	1	0
J	0	1	0	0	1	0	1	0	0	0	1	0	1	1	1	1	1
K	1	1	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0
L	0	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1
M	1	1	0	0	1	1	0	1	0	0	1	1	0	0	0	1	0
N	1	1	0	0	1	1	1	0	0	0	1	1	0	0	0	1	1
O	0	1	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0
P	1	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1
Q	0	1	0	1	0	0	0	1	0	0	1	1	0	0	1	1	0
R	0	1	0	1	0	0	1	0	0	0	1	1	0	0	1	1	1
S	1	1	0	1	0	0	1	1	0	0	1	1	0	1	0	0	0
T	0	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	1
U	1	1	0	1	0	1	0	1	0	0	1	1	0	1	0	1	0
V	1	1	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1
W	0	1	0	1	0	1	1	1	0	0	1	1	0	1	1	0	0
X	0	1	0	1	1	0	0	0	0	0	1	1	0	1	1	0	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
Y	1	1	0	1	1	0	0	1	0	0	1	1	0	1	1	1	0
Z	1	1	0	1	1	0	1	0	0	0	1	1	0	1	1	1	1
SP	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	1	1	1	0	0	0	1
1	0	0	1	1	0	0	0	1	0	0	1	1	1	0	0	1	0
2	0	0	1	1	0	0	1	0	0	0	1	1	1	0	0	1	1
3	1	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	0
4	0	0	1	1	0	1	0	0	0	0	1	1	1	0	1	0	1
5	1	0	1	1	0	1	0	1	0	0	1	1	1	0	1	1	0
6	1	0	1	1	0	1	1	0	0	0	1	1	1	0	1	1	1
7	0	0	1	1	0	1	1	1	0	0	1	1	1	1	0	0	0
8	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	1
9	1	0	1	1	1	0	0	1	0	0	1	1	1	1	0	1	0
SP	0	0	1	0	0	0	0	0	0	0	1	1	1	1	0	1	1
a	0	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0
b	0	1	1	0	0	0	1	0	0	0	1	1	1	1	1	0	1
c	1	1	1	0	0	0	1	1	0	0	1	1	1	1	1	1	0
d	0	1	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1
e	1	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0
f	1	1	1	0	0	1	1	0	0	1	0	0	0	0	0	0	1
g	0	1	1	0	0	1	1	1	0	1	0	0	0	0	0	1	0
h	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0	1	1
i	1	1	1	0	1	0	0	1	0	1	0	0	0	0	1	0	0
j	1	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0	1
k	0	1	1	0	1	0	1	1	0	1	0	0	0	0	1	1	0
l	1	1	1	0	1	1	0	0	0	1	0	0	0	0	1	1	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
m	0	1	1	0	1	1	0	1	0	1	0	0	0	1	0	0	0
n	0	1	1	0	1	1	1	0	0	1	0	0	0	1	0	0	1
o	1	1	1	0	1	1	1	1	0	1	0	0	0	1	0	1	0
p	0	1	1	1	0	0	0	0	0	1	0	0	0	1	0	1	1
q	1	1	1	1	0	0	0	1	0	1	0	0	0	1	1	0	0
r	1	1	1	1	0	0	1	0	0	1	0	0	0	1	1	0	1
s	0	1	1	1	0	0	1	1	0	1	0	0	0	1	1	1	0
t	1	1	1	1	0	1	0	0	0	1	0	0	0	1	1	1	1
u	0	1	1	1	0	1	0	1	0	1	0	0	1	0	0	0	0
v	0	1	1	1	0	1	1	0	0	1	0	0	1	0	0	0	1
w	1	1	1	1	0	1	1	1	0	1	0	0	1	0	0	1	0
x	1	1	1	1	1	0	0	0	0	1	0	0	1	0	0	1	1
y	0	1	1	1	1	0	0	1	0	1	0	0	1	0	1	0	0
z	0	1	1	1	1	0	1	0	0	1	0	0	1	0	1	0	1
SP	0	0	1	0	0	0	0	0	0	1	0	0	1	0	1	1	0
				S	a	m	e						T	h	r	u	
SP	0	0	1	0	0	0	0	0	0	1	0	1	0	0	1	0	1
ETB	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1	1	0
(BP)	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1
STX	1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0	0
DEL	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	0	1
NUL	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
SOH	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1
STX	0	0	0	0	0	0	1	0	0	1	0	1	0	1	1	0	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA BINARY BITS								ADDRESS BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
ETX	1	0	0	0	0	0	1	1	0	1	0	1	0	1	1	0	1
	1	0	0	0	0	1	0	0	0	1	0	1	0	1	1	1	0
ENQ	1	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1
ACK 1	1	0	0	0	0	1	1	0	0	1	0	1	1	0	0	0	0
INV	0	0	0	0	0	1	1	1	0	1	0	1	1	0	0	0	1
	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	1	0
	1	0	0	0	1	0	0	1	0	1	0	1	1	0	0	1	1
LF	1	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0
	0	0	0	0	1	0	1	1	0	1	0	1	1	0	1	0	1
FF	1	0	0	0	1	1	0	0	0	1	0	1	1	0	1	1	0
CR	0	0	0	0	1	1	0	1	0	1	0	1	1	0	1	1	1
SO	0	0	0	0	1	1	1	0	0	1	0	1	1	1	0	0	0
SI	1	0	0	0	1	1	1	1	0	1	0	1	1	1	0	0	1
	0	0	0	1	0	0	0	0	0	1	0	1	1	1	0	1	0
REP	1	0	0	1	0	0	0	1	0	1	0	1	1	1	0	1	1
RM	1	0	0	1	0	0	1	0	0	1	0	1	1	1	1	0	0
	0	0	0	1	0	0	1	1	0	1	0	1	1	1	1	0	1
DC4	1	0	0	1	0	1	0	0	0	1	0	1	1	1	1	1	0
NAK	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1
SYN	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	0
ETB	1	0	0	1	0	1	1	1	0	1	1	0	0	0	0	0	1
CAN	1	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	0
EM	0	0	0	1	1	0	0	1	0	1	1	0	0	0	0	1	1
	0	0	0	1	1	0	1	0	0	1	1	0	0	0	1	0	0
	1	0	0	1	1	0	1	1	0	1	1	0	0	0	1	0	1
ACK 2	0	0	0	1	1	1	0	0	0	1	1	0	0	0	1	1	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
	1	0	0	1	1	1	0	1	0	1	1	0	0	0	1	1	1
WBT	1	0	0	1	1	1	1	0	0	1	1	0	0	1	0	0	0
	0	0	0	1	1	1	1	1	0	1	1	0	0	1	0	0	1
SP	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0
!	1	0	1	0	0	0	0	1	0	1	1	0	0	1	0	1	1
"	1	0	1	0	0	0	1	0	0	1	1	0	0	1	1	0	0
#	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1	0	1
$	1	0	1	0	0	1	0	0	0	1	1	0	0	1	1	1	0
%	0	0	1	0	0	1	0	1	0	1	1	0	0	1	1	1	1
&	0	0	1	0	0	1	1	0	0	1	1	0	1	0	0	0	0
'	1	0	1	0	0	1	1	1	0	1	1	0	1	0	0	0	1
(	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	1	0
)	0	0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1
*	0	0	1	0	1	0	1	0	0	1	1	0	1	0	1	0	0
+	1	0	1	0	1	0	1	1	0	1	1	0	1	0	1	0	1
,	0	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1	0
-	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1	1	1
.	1	0	1	0	1	1	1	0	0	1	1	0	1	1	0	0	0
/	0	0	1	0	1	1	1	1	0	1	1	0	1	1	0	0	1
:	1	0	1	1	1	0	1	0	0	1	1	0	1	1	0	1	0
;	0	0	1	1	1	0	1	1	0	1	1	0	1	1	0	1	1
<	1	0	1	1	1	1	0	0	0	1	1	0	1	1	1	0	0
=	0	0	1	1	1	1	0	1	0	1	1	0	1	1	1	0	1
>	0	0	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
?	1	0	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1
'	0	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA BINARY BITS								ADDRESS BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
[	0	1	0	1	1	0	1	1	0	1	1	1	0	0	0	0	1
~	1	1	0	1	1	1	0	0	0	1	1	1	0	0	0	1	0
]	0	1	0	1	1	1	0	1	0	1	1	1	0	0	0	1	1
^	0	1	0	1	1	1	1	0	0	1	1	1	0	0	1	0	0
DEL	1	1	0	1	1	1	1	1	0	1	1	1	0	0	1	0	1
@	1	1	1	0	0	0	0	0	0	1	1	1	0	0	1	1	0
{	1	1	1	1	1	0	1	1	0	1	1	1	0	0	1	1	1
¬	0	1	1	1	1	1	0	0	0	1	1	1	0	1	0	0	0
}	1	1	1	1	1	1	0	1	0	1	1	1	0	1	0	0	1
|	1	1	1	1	1	1	1	0	0	1	1	1	0	1	0	1	0
SP	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0	1	1
	S a m e								T h r u								
SP	1	0	1	0	0	0	0	0	0	1	1	1	1	0	1	0	0
LF	0	0	0	0	1	0	1	0	0	1	1	1	1	0	1	0	1
N	1	1	0	0	1	1	1	0	0	1	1	1	1	0	1	1	0
N	1	1	0	0	1	1	1	0	0	1	1	1	1	0	1	1	1
N	1	1	0	0	1	1	1	0	0	1	1	1	1	1	0	0	0
N	1	1	0	0	1	1	1	0	0	1	1	1	1	1	0	0	1
ETX	0	0	0	0	0	0	1	1	0	1	1	1	1	1	0	1	0
(BP)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1
SOH	1	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0
(Select)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
Z	1	1	0	1	1	0	1	0	0	1	1	1	1	1	1	1	0
C	0	1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1
Z	1	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA BINARY BITS								ADDRESS BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
C	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0	0	1
J	0	1	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0
T	0	1	0	1	0	1	0	0	1	0	0	0	0	0	0	1	1
A	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0
1	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1
2	0	0	1	1	0	0	1	0	1	0	0	0	0	0	1	1	0
3	1	0	1	1	0	0	1	1	1	0	0	0	0	0	1	1	1
SP	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0
	S a m e								T h r u								
SP	0	0	1	0	0	0	0	0	1	0	0	0	1	1	1	1	0
(	1	0	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1
T	0	1	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0
H	1	1	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1
I	0	1	0	0	1	0	0	1	1	0	0	1	0	0	0	1	0
S	1	1	0	1	0	0	1	1	1	0	0	1	0	0	0	1	1
SP	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	0	0
I	0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
S	1	1	0	1	0	0	1	1	1	0	0	1	0	0	1	1	0
SP	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1
A	1	1	0	0	0	0	0	1	1	0	0	1	0	1	0	0	0
SP	0	0	1	0	0	0	0	0	1	0	0	1	0	1	0	0	1
T	0	1	0	1	0	1	0	0	1	0	0	1	0	1	0	1	0
E	0	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1
S	1	1	0	1	0	0	1	1	1	0	0	1	0	1	1	0	0
T	0	1	0	1	0	1	0	0	1	0	0	1	0	1	1	0	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
SP	0	0	1	0	0	0	0	0	1	0	0	1	0	1	1	1	0
M	1	1	0	0	1	1	0	1	1	0	0	1	0	1	1	1	1
E	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0
S	1	1	0	1	0	0	1	1	1	0	0	1	1	0	0	0	1
S	1	1	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0
A	1	1	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
G	1	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	0
E	0	1	0	0	0	1	0	1	1	0	0	1	1	0	1	0	1
)	0	0	1	0	1	0	0	1	1	0	0	1	1	0	1	1	0
SP	0	0	1	0	0	0	0	0	1	0	0	1	1	0	1	1	1
			S	a	m	e						T	h	r	u		
SP	0	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	1
ETB	0	0	0	1	0	1	1	1	1	0	1	0	0	1	1	1	0
(BP)	0	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	1
STX	1	0	0	0	0	0	1	0	1	0	1	0	1	0	0	0	0
DEL	1	1	1	1	1	1	1	1	1	0	1	0	1	0	0	0	1
R	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1	0
C	0	1	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1
C	0	1	0	0	0	0	1	1	1	0	1	0	1	0	1	0	0
M	1	1	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1
D	1	1	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
H	1	1	0	0	1	0	0	0	1	0	1	0	1	0	1	1	1
A	1	1	0	0	0	0	0	1	1	0	1	0	1	1	0	0	0
B	1	1	0	0	0	0	1	0	1	0	1	0	1	1	0	0	1
SP	0	0	1	0	0	0	0	0	1	0	1	0	1	1	0	1	0
Y	1	1	0	1	1	0	0	1	1	0	1	0	1	1	0	1	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
W	0	1	0	1	0	1	1	1	1	0	1	0	1	1	1	0	0
N	1	1	0	0	1	1	1	0	1	0	1	0	1	1	1	0	1
A	1	1	0	0	0	0	0	1	1	0	1	0	1	1	1	1	0
D	1	1	0	0	0	1	0	0	1	0	1	0	1	1	1	1	1
X	0	1	0	1	1	0	0	0	1	0	1	1	0	0	0	0	0
SP	0	0	1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	0	1	0
2	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0	1	1
3	1	0	1	1	0	0	1	1	1	0	1	1	0	0	1	0	0
4	0	0	1	1	0	1	0	0	1	0	1	1	0	0	1	0	1
SP	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	0
1	0	0	1	1	0	0	0	1	1	0	1	1	0	0	1	1	1
2	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0	0	0
3	1	0	1	1	0	0	1	1	1	0	1	1	0	1	0	0	1
1	0	0	1	1	0	0	0	1	1	0	1	1	0	1	0	1	0
2	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0	1	1
3	1	0	1	1	0	0	1	1	1	0	1	1	0	1	1	0	0
4	0	0	1	1	0	1	0	0	1	0	1	1	0	1	1	0	1
-	1	0	1	0	1	1	0	1	1	0	1	1	0	1	1	1	0
M	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	1	1
N	1	1	0	0	1	1	1	0	1	0	1	1	1	0	0	0	0
S	1	1	0	1	0	0	1	1	1	0	1	1	1	0	0	0	1
H	1	1	0	0	1	0	0	0	1	0	1	1	1	0	0	1	0
-	1	0	1	0	1	1	0	1	1	0	1	1	1	0	0	1	1
-	1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	0	0
Y	1	1	0	1	1	0	0	1	1	0	1	1	1	0	1	0	1

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA BINARY BITS								ADDRESS BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
E	0	1	0	0	0	1	0	1	1	0	1	1	1	0	1	1	0
X	0	1	0	1	1	0	0	0	1	0	1	1	1	0	1	1	1
A	1	1	0	0	0	0	0	1	1	0	1	1	1	1	0	0	0
D	1	1	0	0	0	1	0	0	1	0	1	1	1	1	0	0	1
X	0	1	0	1	1	0	0	0	1	0	1	1	1	1	0	1	0
.	1	0	1	0	1	1	1	0	1	0	1	1	1	1	0	1	1
SP	0	0	1	0	0	0	0	0	1	0	1	1	1	1	1	0	0
	S a m e								T h r u								
SP	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	1
ETB	0	0	0	1	0	1	1	1	1	1	0	1	0	0	0	1	0
(BP)	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	1	1
STX	1	0	0	0	0	0	1	0	1	1	0	1	0	0	1	0	0
DEL	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1
SP	0	0	1	0	0	0	0	0	1	1	0	1	0	0	1	1	0
!	1	0	1	0	0	0	0	1	1	1	0	1	0	0	1	1	1
"	1	0	1	0	0	0	1	0	1	1	0	1	0	1	0	0	0
#	0	0	1	0	0	0	1	1	1	1	0	1	0	1	0	0	1
$	1	0	1	0	0	1	0	0	1	1	0	1	0	1	0	1	0
%	0	0	1	0	0	1	0	1	1	1	0	1	0	1	0	1	1
&	0	0	1	0	0	1	1	0	1	1	0	1	0	1	1	0	0
'	1	0	1	0	0	1	1	1	1	1	0	1	0	1	1	0	1
(	1	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0
)	0	0	1	0	1	0	0	1	1	1	0	1	0	1	1	1	1
*	0	0	1	0	1	0	1	0	1	1	0	1	1	0	0	0	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
+	1	0	1	0	1	0	1	1	1	1	0	1	1	0	0	0	1
,	0	0	1	0	1	1	0	0	1	1	0	1	1	0	0	1	0
-	1	0	1	0	1	1	0	1	1	1	0	1	1	0	0	1	1
.	1	0	1	0	1	1	1	0	1	1	0	1	1	0	1	0	0
/	0	0	1	0	1	1	1	1	1	1	0	1	1	0	1	0	1
:	1	0	1	1	1	0	1	0	1	1	0	1	1	0	1	1	0
;	0	0	1	1	1	0	1	1	1	1	0	1	1	0	1	1	1
<	1	0	1	1	1	1	0	0	1	1	0	1	1	1	0	0	0
=	0	0	1	1	1	1	0	1	1	1	0	1	1	1	0	0	1
>	0	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	0
?	1	0	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1
\	0	1	0	0	0	0	0	0	1	1	0	1	1	1	1	0	0
[	0	1	0	1	1	0	1	1	1	1	0	1	1	1	1	0	1
~	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	1	0
]	0	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1	1
^	0	1	0	1	1	1	1	0	1	1	1	0	0	0	0	0	0
_	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	1
@	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
{	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	1	1
`	0	1	1	1	1	1	0	0	1	1	1	0	0	0	1	0	0
}	1	1	1	1	1	1	0	1	1	1	1	0	0	0	1	0	1
|	1	1	1	1	1	1	1	0	1	1	1	0	0	0	1	1	0
0	1	0	1	1	0	0	0	0	1	1	1	0	0	0	1	1	1
1	0	0	1	1	0	0	0	1	1	1	1	0	0	1	0	0	0
2	0	0	1	1	0	0	1	0	1	1	1	0	0	1	0	0	1
3	1	0	1	1	0	0	1	1	1	1	1	0	0	1	0	1	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA								ADDRESS								
	BINARY BITS								BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
4	0	0	1	1	0	1	0	0	1	1	1	0	0	1	0	1	1
5	1	0	1	1	0	1	0	1	1	1	1	0	0	1	1	0	0
6	1	0	1	1	0	1	1	0	1	1	1	0	0	1	1	0	1
7	0	0	1	1	0	1	1	1	1	1	1	0	0	1	1	1	0
8	0	0	1	1	1	0	0	0	1	1	1	0	0	1	1	1	1
9	1	0	1	1	1	0	0	1	1	1	1	0	1	0	0	0	0
A	1	1	0	0	0	0	0	1	1	1	1	0	1	0	0	0	1
B	1	1	0	0	0	0	1	0	1	1	1	0	1	0	0	1	0
C	0	1	0	0	0	0	1	1	1	1	1	0	1	0	0	1	1
D	1	1	0	0	0	1	0	0	1	1	1	0	1	0	1	0	0
E	0	1	0	0	0	1	0	1	1	1	1	0	1	0	1	0	1
F	0	1	0	0	0	1	1	0	1	1	1	0	1	0	1	1	0
G	1	1	0	0	0	1	1	1	1	1	1	0	1	0	1	1	1
H	1	1	0	0	1	0	0	0	1	1	1	0	1	1	0	0	0
I	0	1	0	0	1	0	0	1	1	1	1	0	1	1	0	0	1
J	0	1	0	0	1	0	1	0	1	1	1	0	1	1	0	1	0
K	1	1	0	0	1	0	1	1	1	1	1	0	1	1	0	1	1
L	0	1	0	0	1	1	0	0	1	1	1	0	1	1	1	0	0
M	1	1	0	0	1	1	0	1	1	1	1	0	1	1	1	0	1
N	1	1	0	0	1	1	1	0	1	1	1	0	1	1	1	1	0
O	0	1	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1
P	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0
Q	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0	0	1
R	0	1	0	1	0	0	1	0	1	1	1	1	0	0	0	1	0
S	1	1	0	1	0	0	1	1	1	1	1	1	0	0	0	1	1
T	0	1	0	1	0	1	0	0	1	1	1	1	0	0	1	0	0

Table 2-1. Contents of AIUTE Transmitter ROM (Cont.)

CHARACTER	DATA BINARY BITS								ADDRESS BINARY BITS								
	8	7	6	5	4	3	2	1	9	8	7	6	5	4	3	2	1
U	1	1	0	1	0	1	0	1	1	1	1	1	0	0	1	0	1
V	1	1	0	1	0	1	1	0	1	1	1	1	0	0	1	1	0
W	0	1	0	1	0	1	1	1	1	1	1	1	0	0	1	1	1
X	0	1	0	1	1	0	0	0	1	1	1	1	0	1	0	0	0
Y	1	1	0	1	1	0	0	1	1	1	1	1	0	1	0	0	1
Z	1	1	0	1	1	0	1	0	1	1	1	1	0	1	0	1	0
SP	0	0	1	0	0	0	0	0	1	1	1	1	0	1	0	1	1
	S a m e								T h r u								
SP	0	0	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0
LF	0	0	0	0	1	0	1	0	1	1	1	1	1	0	0	0	1
N	1	1	0	0	1	1	1	0	1	1	1	1	1	0	0	1	0
N	1	1	0	0	1	1	1	0	1	1	1	1	1	0	0	1	1
N	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1	0	0
N	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1	0	1
ETX	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
(BP)	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1

adjoining pair. These characters direct a receiving terminal to take action. The transmit control characters are REP (reply) and CAN (cancel). Transmit control characters can be sent between blocks of a message or after the 82nd character of a block in continuous mode. The special control characters are EM (end of medium) and SYN (synchronous idle). The EM is used only with magnetic tape messages and is sent following the last text character of a block with 79 or fewer text characters. The SYN is sent continuously whenever the transmitting terminal is not sending a block or a control character sequence. Control characters received at the AIUTE receiver section are not stored in the RAM, but processed separately and displayed on the panel. Control characters transmitted by the AIUTE transmitter section are contained in a 32 by 8-bit ROM. Control character requests from the AIUTE receiver and in the AIUTE transmitter are decoded to address this ROM for the proper control character.

2-9. GENERAL DESCRIPTION.

2-10. The AIUTE simulates a remote terminal to exercise the AIU transmitter and receiver for test. Initially, DCT operating procedures are performed to transmit or receive a one, two, or three block message. To test the AIU transmitter, a message is sent from an input peripheral subsystem to the AIU input channel and then transmitted to the AIUTE receiver station. The receiver writes the message in its RAM. The operator then examines the message on AIUTE panel indicators and determines if the AIU properly transmitted the message. To test the AIU receiver, the message is read from the AIUTE transmitter section ROM or RAM. The ROM contains messages loaded by the manufacturer at the factory. The RAM must be loaded with a message by operator switch action at the panel before test. Also, to use either memory, a select character must first be loaded in the RAM at memory location 00000001. The message is transmitted from the AIUTE transmitter to the AIU receiver and then sent to an output peripheral device on the AIU output channel and/or to the output monitor printer on the AIU output monitor channel. The message can then be examined to determine if the AIU properly received the message. The AIUTE receiver and transmitter data is transferred bit serial and character serial between the AIUTE and the AIU. Each bit is transferred on occurrence of the Tx and Rx clock. The AIUTE is capable of operating in half or full duplex mode at selectable transfer rates of 600, 1200, 2400, or 4800 baud. The AIUTE is also capable of operating in a self test mode. Figure 2-1 shows a timing diagram and table 2-2 lists and describes the clock time events for the AIUTE. The following paragraphs describe timing and synchronization and the AIUTE receiver and transmitter sections.

2-11. TIMING AND SYNCHRONIZATION. Prior to the exchange of data, timing and character synchronization must be established. For clock step operation (bit or character mode), the AIUTE clock is controlled by the STEP switch on the panel. For automatic operation (block, message, or continuous mode), the AIUTE clock is started upon power-up and master clear. The AIUTE clock provides the Tx and Rx clock to the AIU and the control clock for AIUTE timing. The control clock controls bit loading for the receiver serial input register and bit transmitting for the transmitter serial output register. The control clock also controls the transmit timing (TT). TT0 through TT7 controls the processing of characters in the AIUTE receiver and transmitter. When the

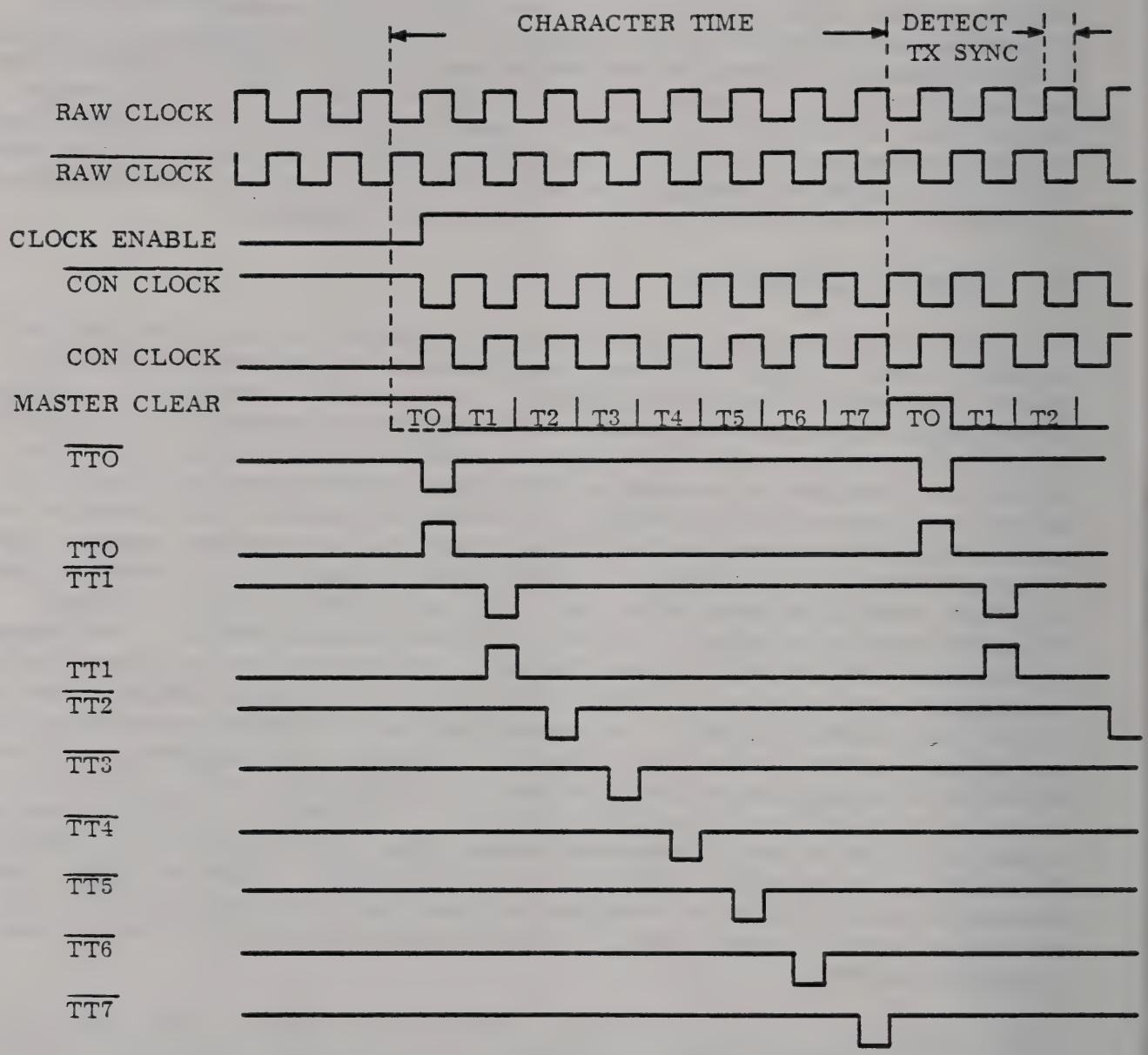


Figure 2-1. AIUTE Timing Diagram

Table 2-2. AIUTE Clock Time Events

CLOCK TIME	RECEIVER	TRANSMITTER
TT0	• Clock input holding register to load character assembled. • Clear answer FF.	• Load serial output register with selected character. • Set character step FF. • Clock block parity generator register.
TT1	• Clock start of block FF. • Clock 2nd frame FF. • Set NACK request FF. • Set EXT received FF.	• Increment address register. • Increment character counter.
TT2	• Clear text FF. • Gate 2Rx. • Clock block parity check register.	• Clock control character count. • Clear run FF.
TT3	• Set block in progress FF. • Set NACK request FF. • Load control character reg.	• Clear request register.
TT4	• Clear request register.	
TT5	• Enable write RAM. • Clock enable check FF. • Clock end of block FF.	• Clock request register.
TT6	• Increment address register. • Increment character counter. • Clock ACK request FF.	• Set run FF.
TT7	• Set text FF. • Clear block in progress FF. • Load control character request.	• Select A and/or B. • Set send block parity FF.

control clock has assembled a character in the receiver serial input register, the outputs are sampled to detect a SYN character. When a SYN character is detected, a sync reset signal is sent to the transmitter to reset the transmit timing. At TT0, the receiver holding register is loaded with the SYN character. The character is checked for even parity and decoded to light a SYNC indicator on the panel. The receiver continues processing SYN characters received from the AIU and is in synchronous idle. At TT7, the transmitter selects the SYN character read from the control character ROM. At TT0, the SYN character is loaded into the transmitter serial output register and transmitted to the AIU by the control clock. The transmitter continues processing SYN characters read from the control character ROM and is in synchronous idle. When the operator presses the CAN switch on the AIU panel, the CAN control character sequence is received at the AIUTE receiver. At TT0, the first CAN character is loaded into the receiver holding register and checked for even parity. The second CAN character is processed at the next TT0. At TT2, the two CAN characters are recognized as a transmit control character sequence and the answer FF is set. At TT3, the control character register is loaded to light a CAN indicator on the panel. At TT6, the send ACK 2 signal is active at the receiver control character request register. At TT7, the register is loaded and an ACK 2 request is sent to the transmitter. At TT0, the receiver processes another SYN character and clears the answer FF. At TT7, the transmitter selects the first ACK 2 control character, and at TT0 loads the serial output register. At TT7, the second ACK 2 control character is selected and loaded into the serial output register at TT0. At TT2, the transmitter sends a 2 sent signal to the receiver, and at TT4 the control character request register in the receiver is cleared. At TT7, the transmitter selects a SYN character and resumes processing SYN characters to the AIU. The AIUTE receiver is now character-synchronized with the AIU transmitter. When the operator presses the CAN switch on the AIUTE panel and TT5 occurs, the transmitter control character ROM is addressed for the CAN character. The CAN character is selected at TT7 and processed at TT0 as previously described. When two CAN characters have been transmitted, the AIU returns the ACK 2 control character sequence to the AIUTE receiver. The control character sequence is processed as previously described and lights the ACK 2 indicator on the panel. The AIUTE receiver continues to process SYN characters from the AIU. The AIUTE transmitter is now character-synchronized with the AIU receiver. After character synchronization has been established, the receiver is ready to accept the first framing character of a message or another control character. Also, the transmitter is ready to transmit the first framing character of a message or another control character.

2-12. RECEIVER SECTION GENERAL DESCRIPTION. The receiver section has the capability for automatic, clock step, or self test operation. For automatic operation, one block, one three-block message, or continuous three-block messages are received from the AIU. For clock step operation, one bit or character at a time is received from the AIU. The MODE SELECT switch on the panel is set to BLK, MSG, or CONT for automatic operation and BIT or CHAR for clock step operation. Self test operation is enabled by setting the SELF TEST switch on the panel. The following paragraphs describe receiver operations and receiver memory display.

2-13. Receiver Automatic Operation. For automatic operation, the MODE SELECT switch is set to BLK, MSG, or CONT. Also, the BAUD RATE switch position is selected and the TRAN/REC switch is set to REC. When CAN and ACK 2 control character sequences have been exchanged between the AIUTE and the AIU, as previously described, the receiver is character-synchronized and in synchronous idle. When the AIU starts transmitting data, it sends the first framing SOH character. The SOH character is assembled into the receiver serial input register, loaded into the holding register at TT0, and clocked for even parity. If the character is decoded as the SOH character, the SOB (start of block) FF is set at TT1. At TT3, the BIP (block in progress) FF is set to condition a gate for loading the character register. The set output of the BIP FF also conditions a control gate for the address register. At TT5, the SOH character is stored in the first RAM location. At TT6, the control gate to the address register is satisfied to increment the address register and character counter. The second character is assembled and loaded into the holding register at TT0, and at TT1 the second frame FF is set. The set output of the second frame FF conditions gates to the NACK REQ and text FFs. If the character was decoded as a control character, the first character count FF is set at TT2. The character count logic conditions gates to the NACK REQ FF with control character and one RX signal. At TT3, the character is checked to determine if it is a valid even parity select character. If the character is not valid, the NACK REQ FF is set. At TT5, the second character is stored in the second RAM location. At TT6, the address register and character counter are incremented. At TT7, the text FF is set and, if a control character was decoded, the NACK REQ FF is set. The receiver will now accept receive control characters or text characters. The receive control characters are in response to transmit control characters sent from the AIUTE transmitter to the AIU. These characters are decoded by the receiver to light an indicator on the panel. The text characters are processed and stored in the RAM at sequential memory locations. When the character count reaches 082, the AIU sends the third framing ETB character. The ETB character is assembled and loaded into the holding register at TT0. At TT2, the text FF is cleared. When TT3 occurs, the character register is loaded to light the ETB indicator on the panel. At TT5, the ETB character is stored in the RAM and the enable CHK and EOB (end of block) FFs are clocked. The enable CHK FF is in the set state and the EOB FF is reset. The set output of the enable CHK FF conditions a gate to the NACK REQ FF and the block parity check logic. At TT6, the address register and character counter are incremented. When the AIU sends the fourth framing BP (block parity) character, it is loaded into the holding register at TT0. At TT2, the BP character is checked for correct block parity. If a parity error occurred, the gate to the NACK REQ FF is satisfied at TT3 to set the NACK REQ FF. At TT5, the BP character is stored in the RAM and the enable CHK and EOB FFs are clocked. The enable CHK FF is then in the reset state and the EOB FF is set. The set output of the EOB FF satisfies a gate condition at the ACK and WBT FFs and sets the answer FF. At TT6, the address register and character counter are incremented. The address register contains the starting address of the next block and the character counter equals 084. Also, at TT6 the send ACK FF is toggled if the NACK REQ FF is not set and a send ACK 1 signal is active at the character request register. If the NACK FF was set, a send NACK signal is active at the character request register, and if the MODE SELECT switch was set to BLOCK, a send WBT signal is active at the character request register. At TT7, the control character request register is loaded and control character

requests are sent to the AIUTE transmitter. The control character ROM in the AIUTE transmitter is programmed to respond to the requests in priority. The requests in order of descending priority are RM, NAK, WBT, ACK 2, ACK 1, CAN, and REP. The AIU sends SYN characters to maintain character synchronization and the AIUTE transmitter processes the control character sequence with the highest priority. The proper answer to a block is RM, NAK, or ACK (1 or 2). At TT0, the AIUTE transmitter clears the answer FF in the receiver. If the AIU did not receive the proper answer or received the WBT, it sends a REP transmit control character to the AIUTE receiver. The receiver assembles each REP control character of the sequence, loads the input holding register at TT0, and sets the answer FF. This sequence is repeated until the proper answer is returned to the AIU.

2-14. If the MODE SELECT switch was set to BLK, the receiver is in synchronous idle until the CLEAR WBT switch is pressed on the AIUTE panel. The AIU then sends the next message block or a control character. If the MODE SELECT switch was set to MSG, an entire three-block message is automatically received from the AIU. If the MODE SELECT switch was set to CONT, messages are transferred continuously and written in RAM over the previously received messages. If the test message is longer than three blocks, the fourth block fills up the remaining locations in the RAM, and then begins storing over (and destroying) the first block.

2-15. Receiver Clock Step Operation. For clock step operation, the MODE SELECT switch is set to BIT or CHAR and the BAUD RATE switch is set to the desired position. The clock step operation is the same as automatic operation except the transfer of each bit or character is controlled by the STEP switch on the AIUTE panel. The STEP switch controls the AIUTE clock. For BIT, the STEP switch is pressed to transfer one bit from the AIU to the AIUTE receiver. For CHAR, the STEP switch is pressed to transfer one character from the AIU to the AIUTE receiver.

2-16. Receiver Memory Display. To display the content of the receiver RAM, the RECEIVE ADDRESS switches are placed down and the MC switch is pressed to display the contents of the first RAM location on the RECEIVE DATA indicators. The ADV switch is pressed to display the next sequential RAM location. To display a selected RAM location, the RECEIVE ADDRESS switches are set to the desired RAM location and the LOAD switch is pressed.

2-17. Receiver Self Test. For self test operation, the SELF TEST switch on the panel is set and the MC switch is pressed. The receiver and transmitter operate with each other in self test for automatic or clock step operation as previously described. Self test is used for checking out and troubleshooting the AIUTE.

2-18. TRANSMITTER SECTION GENERAL DESCRIPTION. The transmitter section has the capability for automatic, clock step, or self test operation. For automatic operation, one block, one three-block message, or continuous three-block messages are transmitted to the AIU. For clock step operation, one bit or character at a time is transmitted to the AIU. The MODE SELECT switch on the panel is set to BLK, MSG, or CONT for automatic operation and BIT or CHAR for clock step operation. The following paragraphs describe transmitter operations and transmitter memory display.

2-19. Transmitter Automatic Operation. For automatic operation, the MODE SELECT switch is set to BLK, MSG, or CONT. Also, the BAUD RATE switch position is selected and the TRAN/REC switch is set to TRAN. When CAN and ACK 2 control character sequences have been exchanged between the AIUTE and AIU, as previously described, the transmitter is character synchronized and in synchronous idle. To send a message, the ROM or RAM is selected, the MSG Y/R switch is set to Y or R, and the START switch is pressed. At TT6, the run FF is set. The set output of the run FF conditions a gate for incrementing the address register and character count, lights the RUN indicator, and conditions a gate to select data from the first ROM or RAM location. The clear output of the run FF clears the transmit control character request register. At TT7, the memory data is selected for the serial output register. At TT0, the register is loaded with the selected memory data. The data is then transmitted to the AIU by the control clock. At TT1, the address register and character counter increment. With the run FF still set, the select gate is conditioned to select data from the second RAM location. For the second framing (select) character of the first block, the RAM data is selected regardless of the MEM RAM/ROM switch setting. At TT7, the memory data is selected for the serial output register. At TT0, the register is loaded with the selected memory data. At TT1, the address register and character counter are incremented. The transmitter then transmits receive control characters or text characters. The receive control character sequence is in response to a transmit control character sequence sent by the AIU to the AIUTE receiver. When a transmit control character sequence is processed by the receiver, a receive control character request is received by the AIUTE transmitter. The transmitter then addresses the control character ROM for the receive control character. The select gate is not satisfied for ROM or RAM data and the control character ROM data is selected for the serial output register at TT7. When two identical receive control characters have been sent to the AIU, the select gate is conditioned again to select memory data for the serial output register at TT7. The address register and the character counter are not incremented when the transmitter decoding the receive control character sequence. The transmitter continues to transfer text characters until the character counter increments to display 082. The next character read from memory is the third framing ETB character. At TT7, the ETB character is selected for the serial output register and decoded for the ETB character. The decoded ETB character conditions a gate for the third framing character. At TT0, the ETB character is loaded into the serial output register, the block parity generator is clocked, and the third frame FF is set. The set output of the third frame FF conditions a gate to the send BP FF. At TT1, the address register and the character counter are incremented and the select gates are conditioned to select the BP (block parity) character. At TT7, the BP character is selected for the serial output register and the send BP FF is set. The character is decoded to condition gates for clearing the BP generator and for setting the answer out FF. At TT0, the serial output register is loaded with the BP character. At TT1, the address register increments to the starting address of the next message block and the character counter increments to display 084. At TT2, the run FF is cleared, the RUN indicator on the panel turns off, the third frame FF is cleared, and the send BP FF is cleared. The BP generator is then cleared and the answer out FF is set. At TT7, the transmitter selects a SYN character for the serial output register. The transmitter is then in synchronous idle (transmitting SYN characters) until an answer is received from the AIU at the receiver. If a WBT control character sequence is received, the receiver sends a

not set WBT signal to the transmitter. At TT5, the send REP FF is set and at TT7 the REP control character is selected for the serial output register. When two REP control characters have been selected, the send REP FF is cleared by a not clear TCC signal from the receiver. This sequence continues until the block transfer is answered. When the proper answer is received, the answer out FF is cleared.

2-20. If the MODE SELECT switch was set to BLK, the START switch must be pressed to transfer the next block. If the MODE SELECT switch was set to MSG, the run FF is set at TT6 to initiate transfer of the next message block. The remaining two blocks of a three-block message will then be transferred automatically. If the MODE SELECT switch was set to CONT, the three-block message is transferred continuously. The block transfers after the first block are the same as described above except the first framing character is the STX character, the second framing character is the DEL character, and the third framing character is the ETX character for the third block. Also, the second framing character of the second and third blocks is from the memory specified by the MEM RAM/ROM switch setting on the panel.

2-21. Transmitter Clock Step Operation. For clock step operation, the MODE SELECT switch is set to BIT or CHAR and the BAUD RATE switch is set to the desired position. The clock step operation is the same as automatic operation except the transfer of each bit or character is controlled by the STEP switch on the panel. The STEP switch controls the AIUTE clock after the START switch is initially pressed. For BIT, the START switch is initially pressed and then the STEP switch is pressed to transfer each bit for one block. This is repeated for each block transferred. For CHAR, the START switch is initially pressed and then the STEP switch is pressed to transfer each character for one block. This is repeated for each block transferred.

2-22. Transmitter Memory Load and Display. To load the transmitter RAM with the first character, the operator manipulates switches on the AIUTE panel. The MEM RAM/ROM switch is set to RAM, all TRANSMIT ADDRESS switches are set down, the MC switch is pressed, the TRANSMIT DATA switches are set for the SOH character, and the WRITE switch is pressed. The SOH character will be stored at RAM location 00000000 and displayed on the TRANSMIT DATA indicators. To load the next character, the READ switch is pressed to increment the address register, the TRANSMIT DATA switches are set for the proper select character, and the WRITE switch is pressed. The remaining characters of the message are stored in the same manner. To sequentially display the memory contents, the READ switch is pressed. The address indicators will display the address and the data indicators will display the character stored at that address. The address increments each time the READ switch is pressed. The REP and CAN character sequences can also be initiated manually, by pressing the REP or CAN switch on the panel.

2-23. Transmitter Self Test. For self test operation, the SELF TEST switch on the panel is set and the MC switch is pressed. The transmitter and receiver operate with each other in self test for automatic or clock step operation as previously described. Self test is used for checkout and troubleshooting the AIUTE.

2-24. DETAILED DESCRIPTION.

2-25. The AIUTE detailed description covers the receiver and transmitter sections. The logic diagrams for each section are located immediately following this description. The AIUTE interconnection and panel schematic diagrams are also contained in this section. Logic functions are referenced by an alphanumeric component location (UXX). This reference is shown inside the logic symbols on the logic diagram and locates the integrated circuit on the circuit card assembly. In some cases, an English name for the logic function is referenced. This reference also appears on the logic diagram outside the logic symbol.

2-26. RECEIVER SECTION DETAILED DESCRIPTION. Figure 2-2 is a block diagram of the receiver section. The number shown in the lower right corner of a block references a sheet on figure 2-4, which is the logic diagram of the receiver section. The title of each block identifies a functional logic group. The following paragraphs describe the functional groups of logic.

2-27. Receive Logic. The receive logic interfaces the AIUTE receiver with the AIU transmitter, and in self test operation interfaces the AIUTE receiver and transmitter sections. The receive logic, figure 2-4, sheet 2, consists of interface line receivers U80, SYNC INITIATE FF U81, and data input gates U16 and U81. When a sync initiate signal is received from the AIU at the interface line receiver, the AIUTE is initialized and the sync initiate FF is set. The set output of this FF lights the RECEIVE CONTROL/SYNC indicator on the panel. When an Rx data bit is received from the AIU at the interface line receiver, or in self test a Tx data bit, gates U81 and U16 are disabled or satisfied and the data bit is sent to the serial input register.

2-28. Serial Input Register. The serial input register assembles serial input data and outputs parallel data. The serial input register consists of the 8-bit parallel out shift register U35. The serial input register receives serial data from the receive logic and outputs parallel data to the input holding register and sync detect logic. The register is loaded, one bit at a time, by the control clock from the AIUTE transmitter. A master clear at the AIUTE panel or a sync initiate signal from the AIU clears the serial input register.

2-29. Sync Detect and Resync. The sync detect and resync logic detects SYN characters assembled in the serial input register and resets the AIUTE transmitter timing. The sync detect logic U23 and U29 (sh. 2) and sync reset logic U19 and U20 (sh. 3) monitors the SYN characters and provides a sync reset signal to the clock timing generator in the AIUTE transmitter. The outputs of the serial input register are sampled for a SYN character by gates U23 and U29. When a SYN character is detected, a not sync signal is sent to condition the sync reset FF U19. The control clock clocks the FF to trigger one-shot U20. The not sync reset pulse is then sent to the AIUTE transmitter clock timing generator.

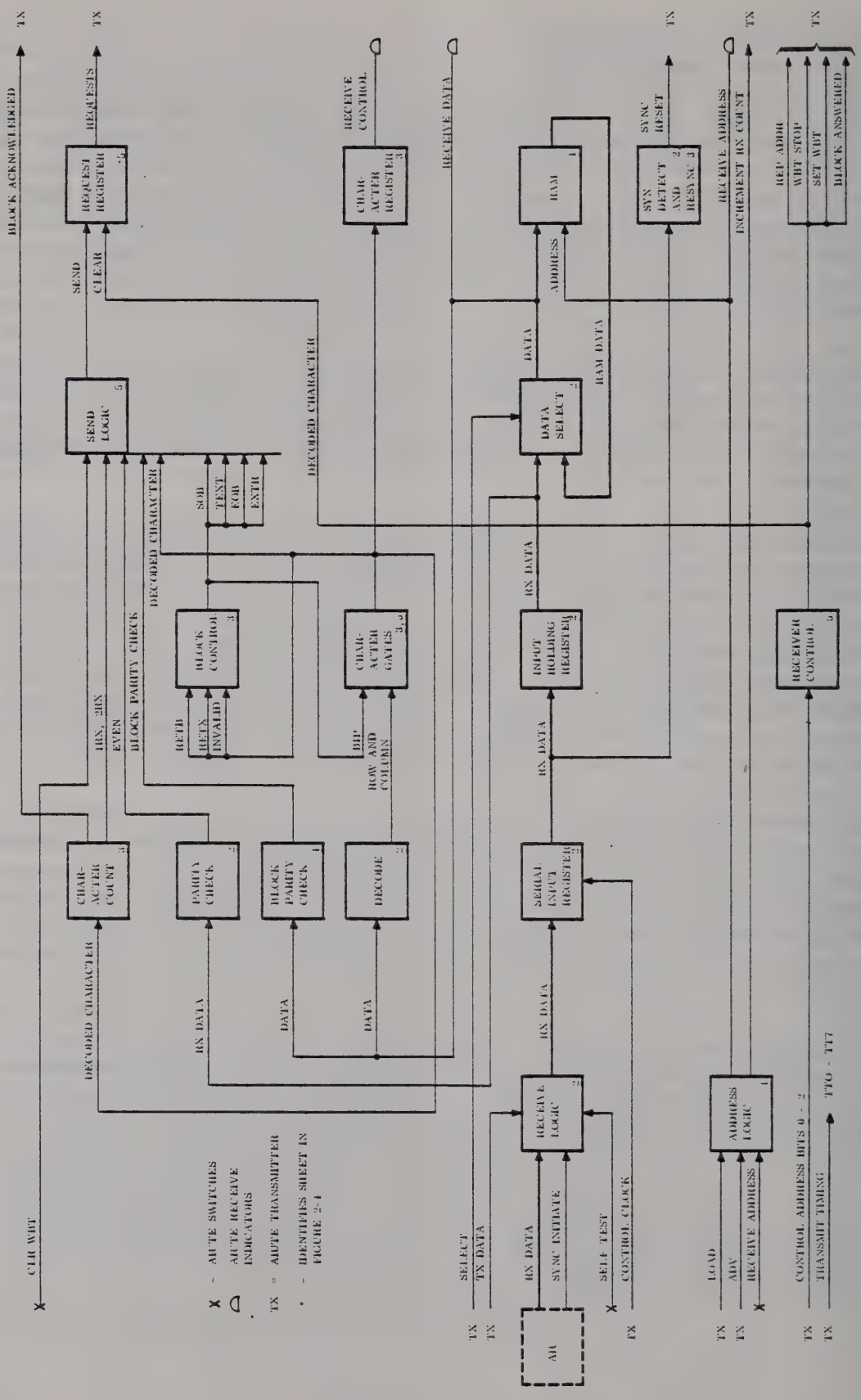


Figure 2-2. Receiver Section Block Diagram

2-30. Input Holding Register. The input holding register holds the character assembled in the serial input register for one character time (TT0 through TT7). The input holding register (sh. 2) consists of eight FFs, U28, U30, U34, and U36. The parallel output of the input shift register is loaded into the input holding register when it is clocked at TT0. The register outputs are then available at the parity check and data select logic. The register is cleared by a master clear or sync initiate signal.

2-31. Parity Check. The parity check logic U53 (sh. 2) checks the character loaded into the input holding register for even parity. If the character is even parity, an even signal is sent to control gates for the NACK request FF in the send logic. The even parity characters consist of control characters or framing characters.

2-32. Receiver Data Select. The receiver data select logic, U52 and U54 (sh. 2), multiplexes the input character or a character read from the RAM. When the ADV switch is pressed on the panel, the character read from the RAM is selected by a select signal from the AIUTE transmitter; otherwise, data loaded into input holding register is selected. The selected data is output to the decode logic, panel indicators, and block parity (BP) check logic.

2-33. Decode. The decode logic decodes the selected input data or RAM data from BCD (binary coded decimal) to decimal for the character gate logic. The decode logic consists of decoders U40, U42, U46, and U48 (sh. 2). The BCD character received from the data select logic is decoded for decimal row and column. The decimal row and column output of the decoder satisfies or conditions gates in the character gate logic.

2-34. Character Gates. The character gates gate the decoded input data or RAM data to the character register or the send logic. The character gates consist of control character gates U43 and U44, first framing character gates U49, and third framing character gates U45 (sh. 3). The character gates also include character error gates U17, U21, and U22 (sh. 5). The character gates receive inputs from the decode logic. When one of the control character gates is satisfied, a receive control character signal is output to the character register, character count logic, and send logic. When one of the first framing character gates is satisfied, a receive first framing character (SOH or STX) signal is sent to the block control logic. When one of the third framing character gates is satisfied, a receive third framing (ETB or ETX) or EM character signal is output to the character register and block control logic or send logic. When the character error gates are satisfied, an invalid select character signal is sent to the send logic.

2-35. Character Register. The character register is loaded with bits from the character gates to light RECEIVE CONTROL indicators on the AIUTE panel. The character register U67, U68, and U69 (sh. 3) receives input from the character gates. Registers U67 and U68 receive input from the control character gates and U69 receives input from the third framing and EM character gates. Input data is loaded into registers U67 and U68 by gates U57 and U63. When a control character sequence has been decoded, the character count logic sends the two Rx signal to gate U57. At TT3, gate U57 is satisfied to satisfy gate U63 and load the register. Gate U63 is also satisfied by a master clear or sync initiate signal. Input data is loaded into register U69 by gates U57, U45,

and U75. When a third framing (ETB or ETX) character or an EM character has been decoded, a BIP signal from the block control logic conditions gate U57, and when TT3 occurs, gate U57 is satisfied to disable gate U45 and satisfy gate U75 to load the register. The output of the character register lights a RECEIVE CONTROL indicator on the panel.

2-36. Receiver Character Count. The receiver character count logic counts control characters received for a control character sequence. The character count logic (sh. 3) consists of gates U49, U50, U55, U56, U61, U63, and count FFs U62. Gate U61 monitors receive control characters. Gates U49 and U55 monitor transmit control characters. When monitor gate U61 or U55 detects a control character, the count FF input gates U55 and U56 are satisfied. When monitor gate U49 detects a control character, a receive transmit control character signal is sent to the send logic to condition a gate for the answer FF. The output of the count FF input gate U55 sets the first count FF at TT2 and the second count FF is reset. Gate U63 is then satisfied to send a one Rx signal to the send logic which conditions a gate for the NACK REQ FF. When the second character is detected and the second count FF is set, gate U63 is satisfied to send a two Rx signal to the send logic and the character register. The two Rx signal conditions a gate to the NACK REQ FF in the send logic and conditions a gate to load the character register. At TT7, gates U50 and U56 are satisfied to clear the character count FFs.

2-37. Receiver Block Control. The receiver block control logic controls the processing of framing and text characters in a block transfer. The block control logic (sh. 3) consists of the SOB, BIP, second frame, text, enable CHK, EOB, and ETX received FFs. When the first framing SOH or STX character is received and the SOB (start of block) FF is clocked at TT1, the SOB FF is set. When set, the SOB FF conditions a gate to the BIP (block in progress) FF and clears the BP check register. The BIP FF is set at TT3. The set output conditions a gate to increment the address register and conditions a gate to load the character register. The second frame FF is set at the next occurrence of TT1. Also, at TT1 the SOB FF is reset. The set output of the second frame FF conditions a gate to the text FF and a gate to the NACK REQ FF in the send logic. At TT7, the text FF is set. The set output at the text FF also conditions gates to the NACK REQ FF in the send logic. The text FF remains set until the third framing ETB or ETX character is received and, at TT2, is then cleared. The text FF is also cleared when a CAN character is received. The enable CHK FF is set at TT5 when the ETB or ETX character is received. The set output of the enable CHK FF also conditions a gate to the NACK REQ FF. The EOB (end of block) FF is set at the next occurrence of TT5 and the enable CHK FF is reset. The reset output of the enable CHK FF conditions a gate to load the character register, conditions a gate to set the SOB FF, and conditions a gate to set itself. The set output of the EOB FF conditions a gate to clear the BIP FF at TT7 and satisfies gates in the send logic. The ETX received FF is set at TT1 when the ETX character is received. The set output satisfies a gate to the WBT FF in the send logic.

2-38. Receiver Address Logic. The receiver address logic provides for sequential RAM addressing and for incrementing the receiver character count. The address logic also provides for loading a RAM address from the panel. The address logic (sh. 4) consists of the RAM address register and gating logic. The address register U82 and U84 operates as a counter for sequential RAM addressing. Also, when the address switches on the panel are set and the LOAD switch is pressed, the register is loaded with the address specified by the address switches. Gates U51, U57, and U75 control sequential memory addressing. If gate U57 is conditioned by a BIP signal, a control character is not being processed, and TT6 occurs, gates U51 and U75 are satisfied to clock the counter and increment the current address by 1. Also, when the ADV switch is pressed, the AIUTE transmitter sends an Rx advance signal which satisfies gates U51 and U75 to clock the counter. For sequential memory addressing, gate U51 also provides an increment Rx count signal to the AIUTE transmitter.

2-39. Receiver RAM. The RAM U58 and U60 (sh. 4) receives input data from the data select logic and is addressed by the address register. The selected input data is written in the RAM at the address specified by the address register. The RAM is enabled for a write operation by control gate U33. This gate is satisfied at TT5 when conditioned by a block in progress signal and when a control character is not being processed. The RAM can also be addressed to display the content of an address location. To display the first memory location, the ADV switch is pressed and then the LOAD switch. For sequential locations, only the ADV switch is pressed. The output of the RAM is then available at the data select logic. The RAM provides storage for 256 8-bit characters. Since one three-block message consists of 252 8-bit characters, the next message will be stored at different memory locations from the first message unless the MC switch is pressed after the first message.

2-40. Block Parity Check Logic. The block parity check logic compares data from the data select logic with the updated status of its BP register. The block parity logic (sh. 4) consists of eight BP register FFs U64, U65, U66, and U71 and two 4-bit comparators. Initially, the BP register is cleared by the SOB signal from the block control logic. The BP register and the comparators each receive BCD characters from the data select logic. The comparators also receive the current status of the BP register. When any of the BP register input bits are a logic 1 and the register is clocked at TT2, the register FF associated with that bit is toggled. The comparator makes a comparison of the BCD input from the data select logic with the current status of the BP register. If a compare is made, the comparator outputs a not BP check signal. This signal disables a gate to the NACK REQ FF in the send logic. If a compare is not made, the BP check signal conditions a gate to the NACK REQ FF. This sequence occurs for each message character in a block, excluding the fourth framing block parity character.

2-41. Receiver Send Logic. The receiver send logic consists of FFs that specify receive control characters for the request register. The send logic (sh. 5) consists of the send RM, send WBT, CLR WBT, NACK REQ, ACK (U9), and answer FFs. The send RM FF is set upon master clear. The set outputs provides a send reject your message signal to the control character request register. The send RM FF is cleared when a CAN control character sequence is received for synchronization. The send WBT

FF is set when gate U1 or U2 is satisfied. Gate U1 is conditioned when the MODE SELECT switch is set to BLK. When an end of block signal is received from the block control logic, the FF is set and a send wait before transmission signal is sent to the request register. Gate U2 is conditioned when the MODE SELECT switch is set to MSG and the SOB signal is received from the block control logic. When the ETX received signal is received from the block control logic, the FF is set and a send wait before transmission signal is sent to the control character request register. The send WBT FF is cleared by the CLR WBT FF. The CLR WBT FF operates with one-shot U20. When the CLR WBT switch on the panel is pressed, the CLR WBT FF is set to trigger one-shot U20. The pulse from one-shot U20 clears the send WBT FF and, when the CLR WBT switch is released, the CLR WBT FF is cleared. The NACK REQ FF is set when gate U2, U3, or U10 is satisfied. There are two U2 gates that control the setting of the NACK REQ FF. One of the U2 gates is conditioned by the enable check signal from the block control logic and the block parity check signal from the BP check logic. When TT3 occurs, gate U2 is satisfied and the NACK REQ FF is set. The other U2 gate is conditioned by the second frame signal from the block control logic and the invalid character signal from the character gates. When TT3 occurs, gate U2 is satisfied and the NACK REQ FF is set. Gate U3 is conditioned by the even signal from the parity check logic and the text signal from the block control logic. If a control character is not being processed and TT3 occurs, the NACK REQ FF is set. Gate U10 is conditioned by the text signal from the block control logic and the one Rx signal from the character count logic. If the first character of a control character sequence is processed and TT1 occurs, the NACK REQ FF is set. The set output of the NACK REQ FF provides a send NACK signal to the control character request register. The NACK REQ FF is cleared when a CAN control character sequence is processed or a SOB signal is received from the block control logic. The ACK FF (U9) is conditioned by gates U14 and U15. Gate U14 is conditioned when the NACK REQ FF is cleared and satisfied when the EOB signal is received from the block control logic. When gate U14 is satisfied, gate U15 is satisfied to condition the ACK FF. At TT6, the FF is toggled to provide a send ACK 1 or send ACK 2 signal to the control character request register. The answer FF is set by gate U14. Gate U14 is conditioned by a received transmit (REP or CAN) control character signal from the character gates. When the two Rx signal is received from the character count logic, the gate is satisfied to set the answer FF. The set output of the answer FF conditions gate U8 to the control character request register. The answer FF is cleared by gate U50 or a master clear. Gate U50 is conditioned by the set output of the answer FF and a clear signal from the receiver control logic. When TT0 occurs, gate U50 is satisfied to clear the answer FF.

2-42. Request Register. The request register receives inputs from the send logic. When the register is loaded, receive control character request signals are sent to the AIUTE transmitter. The request register (sh. 5) consists of the 4-bit latch U13 and the ACK 1 FF U9. The register receives send signals from the send logic and gate U8 loads the 4-bit latch. Gate U8 is conditioned by the clear signal from the receiver control logic and the set output of the answer FF. When TT7 occurs, gate U8 is satisfied to load the latch and disable gate U15. When the latch is loaded, receive control character requests are sent to the AIUTE transmitter. Gate U15 clocks the

ACK 1 FF when it is disabled. If the send acknowledge signal from the send logic is active, the ACK 2 request is sent to the AIUTE transmitter, and the ACK 1 FF is toggled; otherwise, the ACK 1 FF is clocked and the not ACK 1 signal is sent to the AIUTE transmitter. The latch and the ACK 1 FF are cleared at TT4 by a clear signal from the receiver control logic.

2-43. Receiver Control. The receiver control logic interfaces with the AIUTE transmitter to clear the request register and answer FF when a receive control character sequence has been transmitted to the AIU. The logic also sets and clears transmit control character FFs in the AIUTE. The receiver control logic (sh. 5) consists of the decoder U24, WBT STOP FF, and associated gating logic U1, U5, U7, U15, U16, U17, U18, and U22. Character address bits 0, 1, and 2 from the AIUTE transmitter are decoded by decoder U24 and the decimal output is sampled by gates U18 and U22. When gate U18 is disabled and a two sent signal is received from the AIUTE transmitter, gate U17 is conditioned. When TT4 occurs, gate U17 is satisfied to satisfy gate U16 and clear the request register. Also, gates U22 and U5 are disabled to clear the answer FF at TT0. When gate U22 is satisfied, a not reply address signal is sent to the AIUTE transmitter and gate U17 is conditioned. Gate U17 is also conditioned by the two sent signal from the AIUTE transmitter. At TT3, gate U17 is satisfied and a not clear transmit control character signal is sent to the AIUTE transmitter. The WBT STOP FF receives inputs from the character count logic and control character gates. Gate U1 sets the FF and gate U7 clears the FF. Gate U15 is satisfied when a not received wait before transmission signal is received from the control character gates. U15 conditions gate U1 and when the two Rx signal is received from the character count logic, the WBT STOP FF is set. The not set wait before transmission and not wait before transmission stop signals are then sent to the AIUTE transmitter. Gate U7 is conditioned by the received control character signal from the character count logic and the received wait before transmission signal from the control character gates. When the two Rx signals from the control character count logic is received, gate U7 is satisfied to clear the WBT STOP FF. The block answered signal is then sent to the AIUTE transmitter.

2-44. TRANSMITTER SECTION. Figure 2-3 is a block diagram of the transmitter section. The number shown in the lower right corner of a block indicates a sheet in figure 2-5, which is the logic diagram for the transmitter section. The title in each block identifies a functional logic group. The following paragraphs describe the functional groups of logic.

2-45. Clock and Timing. The clock and timing logic controls the exchange of data and control characters between the AIUTE and the AIU, and provides internal timing for the AIUTE. The clock and timing logic, (figure 2-5, sh. 5), consists of one-shots U34, clock counter U40, clock select gate U29, clock gates U64 and U63, line driver U81, timing counter U57, and decoder U75. When the MC (master clear) switch is pressed and one-shots U34 are triggered, clock counter U40 is clocked. The clock counter is a 4-bit ripple-through counter. The output of the counter is selected by the BAUD RATE switch setting. When the count reaches the baud rate selected, the clock select gate U29 is satisfied to disable gate U64. The output of gate U64 then satisfies clock

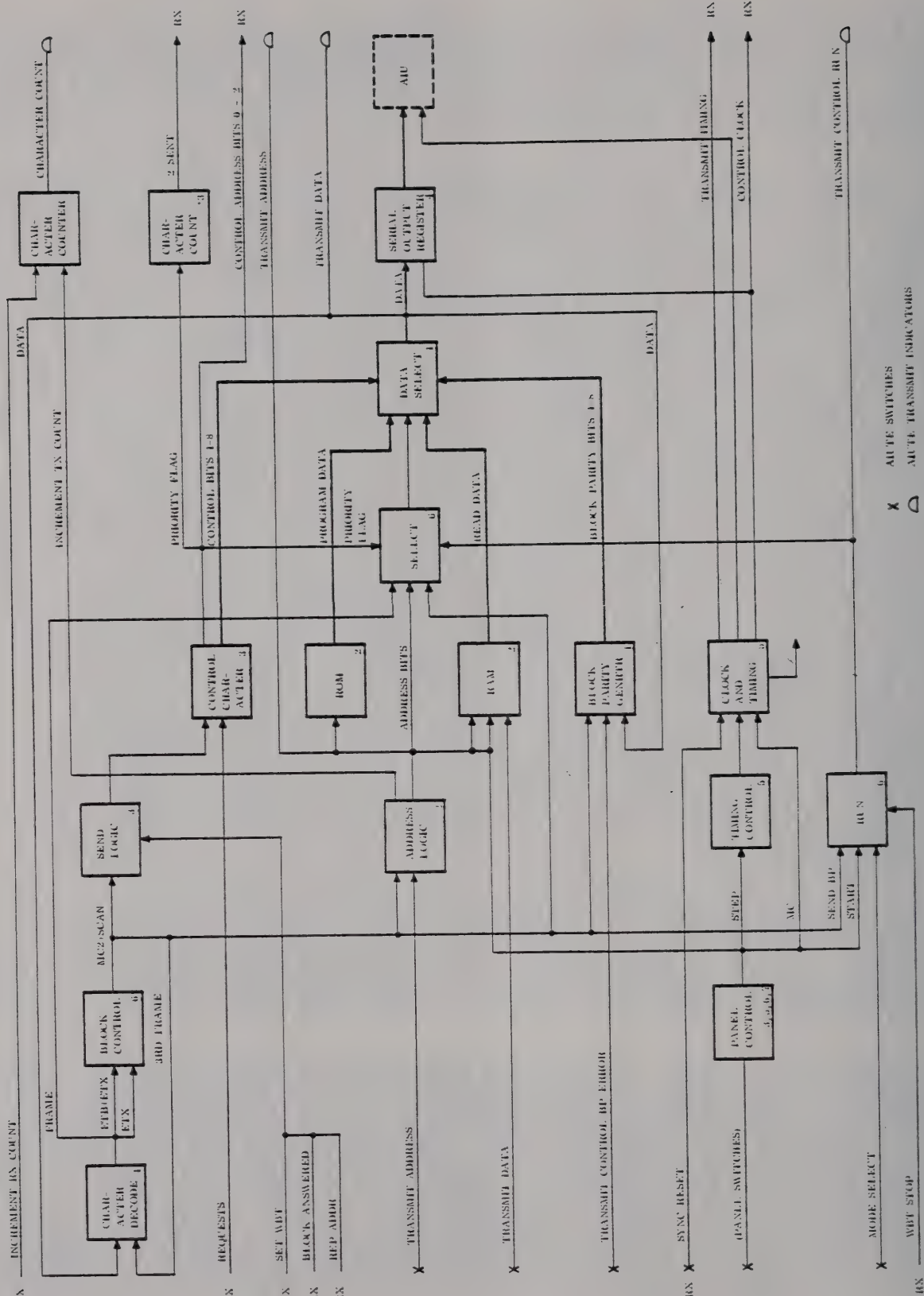


Figure 2-3. Transmitter Section Block Diagram

gate U63 to provide the control clock. The output of gate U64 enables line driver U81 to provide the Tx and Rx clock to the AIU and also forms part of the BCD input to the timing decoder U75. The control clock clocks timing counter U57 to provide the rest of the BCD input to the decoder. The BCD input to decoder U75 is decoded with each clock from gate U64. The output of the decoder provides transmit timing (TT) of TT0 through TT7 sequentially until a sync reset signal is received from the AIUTE receiver. The timing is then restarted to provide character synchronization. The TT provides for transmitter character processing to the serial output register in the transmitter and character processing from the serial input register in the AIUTE receiver. In addition to clocking the timing counter, the control clock outputs serial bits from the serial output register in the transmitter and assembles inputs bits to the serial input register in the AIUTE receiver. The clock select gate, U29, also clocks the control FF in the timing control logic.

2-46. Timing Control. The timing control logic enables the clock and timing logic for automatic operation of the AIUTE. For clock step operation, the timing logic enables and then disables the clock and timing logic each time the STEP switch is pressed. The timing control logic (sh. 5) consists of the ARM and CHAR STEP FFs with control FF U58 and associated gating logic. When the MASTER CLEAR switch is pressed, the control FF is cleared to disable gate U64 in the clock and timing logic. The control FF is then preset if the MODE SELECT switch is set to BLK, MSG, or CONT. The set output of the control FF enables gate U64 in the clock and timing logic to start the TT. If the START switch is pressed, block, message, or continuous operation is allowed since clock gate U64 is enabled by each occurrence of the clock select signal. If the MODE SELECT switch is set to BIT or CHAR, gate U51 is disabled to disable the preset condition at the control FF. When the STEP switch is pressed, gate U76 to the ARM FF is satisfied to set the ARM FF. The set output of the ARM FF conditions gate U67 to the control FF. When the START switch and then the STEP switch in the panel control logic are pressed, gate U67 to the control FF is satisfied. If the MODE SELECT switch was set to BIT, the control FF is toggled to the set condition and one bit is transmitted or received by the control clock. The ARM FF is then cleared and the control FF is reset by the next clock select signal. Each time the STEP switch is pressed, this sequence occurs to transfer one bit and decode the next sequential TT. If the MODE SELECT switch was set to CHAR and the STEP switch is pressed, one bit is transferred and TT0 is output from the decoder. Gate U64 to the CHAR STEP FF is then satisfied to set the FF and the ARM FF is cleared. The set output of the CHAR STEP FF satisfies gate U64 to the control FF to hold the control FF in the set state. When eight bits have been transferred, the CHAR STEP FF is cleared and gate U64 to the control FF is disabled. The next clock select signal resets the control FF to turn off the control clock. Each time the STEP switch is pressed, one 8-bit character is transferred with the decoder outputting TT0 through TT7.

2-47. Run. The run logic controls the operation of the transmitter. The run logic (sh. 6) consists of the start enable, start RQST, and run FFs with associated gating logic. When the START switch in the panel control logic is pressed, the start FF is set to satisfy gate U60 and set the start RQST FF. When the START switch is

released, the start FF is cleared and the start enable FF is set to condition gate U60 for the next start request. The set output of the start RQST FF satisfies gate U42. If a WBT control character sequence has not been received at the AIUTE receiver, gate U30 to the run FF is conditioned by the wait before transmission stop signal from the AIUTE receiver. The output of gate U42 then satisfies gate U30 to set the run FF and clear the ETX sent FF in the block control logic. The set output of the run FF lights an indicator on the panel, conditions gates in the select logic, and conditions a gate in the address logic. Also, when the run FF is set, the clear output clears the send FFs in the request control logic. Gates U35, U41, U47, and U77 maintain the run FF in a set state until a message has been transferred or for continuous operation. The run FF is cleared by master clear, when a WBT control character sequence is received at the AIUTE receiver, or when the send block parity signal from the block control logic conditions gate U42 and TT2 occurs. If the MODE SELECT switch was set to MSG, gate U77 is satisfied to condition gate U47. Gate U47 is also conditioned by the block control logic and the block acknowledged signal from the AIUTE receiver. When TT6 occurs, gate U47 is satisfied to satisfy gate U41, which satisfies gate U42. The run FF is then set to transfer the next block of a message. When an entire message has been transferred, gate U47 is disabled by the block control logic. If the MODE SELECT switch was set to CONT, gate U35 is conditioned. Gate U35 is also conditioned by the block acknowledged signal from the AIUTE receiver. Gate U35 is satisfied at TT6 to maintain the run FF in a set state for continuous operation.

2-48. Transmitter Address Logic. The transmitter address logic provides for sequential RAM or ROM addressing and for incrementing the transmitter character count. The address logic also provides for loading an address from the panel. The address logic (sh. 2) consists of the address register and gating logic. The address register U16 and U18 operates as a counter for sequential RAM or ROM addressing. Also, when the address switches on the panel are set and the LOAD switch is pressed, the register is loaded with the address specified by the address switches. Gate U29, U30, and U35 control sequential memory addressing. Gate U35 is conditioned by the run logic and select logic. Gate U35 is satisfied at TT1 to satisfy gate U30. Gate U30 can also be satisfied by the Tx advance signal from the panel control logic. Gate U30 sends the increment Tx signal to the character counter logic and satisfies gate U29 to increment the address register. The current address is then incremented by 1. The output of the address register addresses both the ROM and RAM memory and enables the proper address indicator drivers U22 and U24 to display the address on the panel. The output of address indicator drivers are sampled by gate U23. When the first memory location is addressed, gate U23 is satisfied to satisfy gate U29. Gate U29 conditions gate U30, and, at TT0, the gate U30 is satisfied to make gate U29. The TA = 1 signal is then sent to the select logic. When the address is other than the first memory location, the not TA = 1 signal is sent to the select logic to force selection of the RAM for data.

2-49. Transmitter ROM and RAM. The transmitter ROM and RAM are addressed by the address register and the selected memory outputs data to the select logic. The transmitter memories consist of the ROM U10 and U12 (sh. 2) and the RAM U4 and U6 (sh. 2). Both memories are addressed by the address register and the selected memory outputs data to the data select logic. The RAM must first be loaded with the second

framing (select) character for the first block of a message if the ROM is to be selected for the message transfer. If the RAM is to be selected, the entire message must be loaded into the RAM by operator switch action at the panel. The ROM is loaded with a message by the manufacturer at the factory. Memory selection is made by the MEM RAM/ROM switch on the panel. If the ROM is selected, the message format must be specified by setting the MSG R-Y switch on the panel. If the RAM is selected, a write enable signal from the panel control logic allows a write operation for the RAM location specified by the address register.

2-50. Select. The select logic selects memory data, a block parity character, or a control character sequence for transfer to the AIU. The select logic (sh. 6) consists of the select A and select B FFs (U78) with associated input and output gating logic. When the select A FF is set, the select A signal is sent to the data select logic to select RAM data. Select B is for ROM data. When both select FFs are set, the block parity character is selected. When both select FFs are reset, the control character is selected. For manual operation of the memories, one of the select FFs is preset to force data selection from the selected memory. Upon master clear, the preset gates U72 are disabled by the absence of a LO signal from the panel control logic. With the RAM selected, one U65 gate is conditioned by the RAM switch signal from the panel and the absence of a not priority flag signal from the control logic. The other U65 gate is disabled by the absence of a priority flag. When the START switch is pressed and the run FF is set, gate U65 is satisfied to make gate U66. At TT7, the select A FF is set. The select A signal is then sent to the data select logic. This sequence is repeated until a priority flag is received from the control logic or the run FF is cleared. Gate U65 is then disabled. If the run FF is not cleared, the other U65 gate is conditioned by the priority flag signal from the control logic and by the RAM switch signal from the panel. If the frame signal is active from the character decode logic, gate U65 is satisfied to satisfy gate U66. When the frame signal drops, both U65 gates are disabled. This allows the data select logic to select the control character only before or after two sequential framing characters. When the priority flag signal drops, the initial U65 gate described above is satisfied to continue RAM data selection. With the ROM selected, one U59 gate is conditioned by the not RAM switch signal from the panel, the absence of a not priority flag signal from the control logic, and the absence of a not TA = 1 signal from the address logic. The other U59 gate is disabled by the absence of a priority flag. When the START switch is pressed and the run FF is set, gate U59 is satisfied to satisfy gate U54. At TT7, the select B FF is set. The select B signal is then sent to the data select logic. When the not TA = 1 signal is received from the address logic, both U59 gates are disabled. Gate U60, which was previously conditioned when the ROM was selected, is satisfied by the TA = 1 signal from the address logic to satisfy gate U66. At TT7, the select A FF is set. The select A signal is then sent to the data select logic. The second framing character is selected from the RAM for both memory selections. When the TA = 1 signal drops, the U59 gate previously described is satisfied to continue the ROM data selection. This sequence is repeated until a not priority flag is received from the control logic or until the run FF is cleared. Gate U59 is then disabled. If the run FF is not cleared, the other U59 gate is conditioned by the priority flag from the control logic, the not RAM switch signal from the panel, and the absence of the not TA = 1 signal from the address logic. If the frame signal is active from the character decode logic, gate U59 is satisfied to make gate U54. When

the frame signal drops, both U59 gates are disabled. This allows the data select logic to select the control character only before or after two sequential framing characters. When a control character is to be selected (both select FFs reset), gate U72 is satisfied. The output of U72 is a MUX 0 signal that is sent to the control logic. A third framing signal from the block control logic satisfies gates U66 and U54. At TT7, both the select A and B signals are sent to the data select logic for the BP character selection. For memory display or RAM write operations from the panel, preset gate U72 is satisfied when the LO signal is received from the control logic. The select A or B signal is then forced and sent to the data select logic.

2-51. Transmitter Data Select. The data select logic (sh. 4) consists of data select multiplexers U2, U3, U8, and U9. The multiplexers receive data from the control character logic, block parity generator, or memories. If either a select A or B signal is received from the select logic, the memory data is selected. If both select A and B signals are received, the block parity character is selected. If both select A and B signals are not received, the control character ROM is selected. The selected data is output to the character decoder, serial output register, block parity generator, and data indicator drivers.

2-52. Character Decode. The character decode logic decodes the selected output data for framing characters and sends control signals to the block control and block parity generator logic. The character decode logic (sh. 4) consists of decoders U32 and U33 with frame FF U50 and associated gating logic. The BCD character input to the decoders is decoded for decimal row and column output to the gating logic. If the decoded character is a framing character, gates U38 and U39 are satisfied to satisfy gate U38 to the frame FF. At TT0, the frame FF is set to send a frame signal to the select logic. If the framing character was the SOH or STX character, gates U51 are conditioned. If the framing character was the ETB or ETX character, the ETB or ETX signals are sent to the block control logic. When the run logic clears the third frame and send BP FFs in the block control logic, gates U51 are satisfied to send clear block parity signals to the block parity generator.

2-53. Serial Output Register. The serial output register logic (sh. 4) consists of the parallel-load 8-bit shift register U27 and interface line driver U81. The register receives input data from the data select logic. At TT0, the selected output data is loaded into the register. The data is shifted out of the register to the interface line driver and the receiver one bit at a time on each occurrence at the control clock. The interface line driver is enabled when the self test switch signal from the panel is not active. The output of the register is then transmitted to the AIU.

2-54. Transmitter Send Logic. The send logic interfaces with the AIUTE receiver to specify transmit control characters. The send logic (sh. 3) consists of the send FFs, request FFs (U61), ANS OUT FF, and associated gating logic. When the not clear block parity 1 signal is received from the character decode logic, the ANS OUT FF is set to condition gate U73. If a not set wait before transmission signal is received from the AIUTE receiver, gate U77 is satisfied to satisfy one of the two U73 gates. The output of gate U73 presets the reply request FF U61, which conditions the send

REP FF. At TT5, the send REP FF is clocked and a send reply request signal is sent to the control character logic. When the reply address signal is received from the AIUTE receiver to satisfy gate U19, gate U49 is conditioned. Gate U49 is satisfied when the two sent signal is received from the character count logic. The output of gate U49 or a master clear signal satisfies gate U41 to clear the reply request FF U61. Master clear also clears the ANS OUT, send CAN, and send REP FFs. The not run signal from the run logic or the not clear transmit control character signal from the AIUTE receiver also clears the send FFs. If a block answered signal is received from the AIUTE receiver, the ANS OUT FF is cleared to condition the other U73 gate and to condition gate U67 to the send CAN FF. When a not set wait before transmission signal is received from the AIUTE receiver to satisfy gate U77, gate U73 is satisfied. The output of gate U73 presets the cancel request FF U61 to satisfy gate U67 and condition the send CAN FF. At TT5, the send CAN FF is clocked and a send cancel request signal is sent to the control character logic. Also, a not scan signal is sent to the block control logic. When the MC switch is pressed, a not master clear 2 + scan signal clears the cancel request FF U61. Request FFs U61 can also be set when clocked by the reply or cancel signal from the panel control logic.

2-55. Control Character. The control character logic prioritizes requests received from the AIUTE receiver and the send logic and outputs control characters to the data select logic. The control character logic (sh. 3) consists of encoder U13 and the control character ROM U1. The encoder receives control character requests from the AIUTE receiver and the send logic. The decimal inputs are encoded for BCD output to address the control character ROM. The encoder decodes the proper priority of requests. When a request is encoded and the ROM is addressed, a not priority flag signal is sent to the character count logic and select logic. Also, control address signals are sent to the AIUTE receiver. The control character addressed in the ROM is output to the data select logic.

2-56. Transmitter Character Count. The character count logic counts the control characters selected for output to the AIU. The character count logic (sh. 3) consists of count FFs U37 and associated gating logic. When the ROM is addressed for a control character, gate U19 is satisfied to condition gate U25 and a priority flag signal is sent to the select logic. When the control character has been selected, a MUX 0 signal from the select logic satisfies gate U25 to satisfy gate U19 and condition the first character count FF. At TT2, the first character count FF is clocked and the set output conditions the second character count FF. When the control character sequence has been selected, the second character count FF is clocked at TT2 and the set output conditions gate U49. Also, a two sent signal is sent to the send logic and the AIUTE receiver. At TT5, gate U49 is satisfied to satisfy gate U67 and to clear the character count FFs. A master clear also satisfies gate U67 to clear the character count FFs.

2-57. Transmitter Block Control. The block control logic controls the processing of block characters in a block transfer. The block control logic (sh. 6) consists of the ETX sent, third frame, and send BP FFs with associated gating logic. When the ETX and ETB+ETX signals are received from the character decode logic, gates U46 to the ETX sent and third frame FFs are conditioned. Gates U46 are also conditioned when

the send BP FF is in a cleared state. At TT0, gates U46 are satisfied to set the ETX send and third frame FFs. The set output of the ETX sent FF conditions gate U42 and the set output of the third frame FF conditions gate U48. The clear output of the ETX sent FF disables a gate in the run logic to prevent automatic setting the run FF. The clear output of the third frame FF sends a third frame signal to the select logic to select the BP character. At TT7, gate U48 is satisfied to set the send BP FF. The set output provides a send BP signal to the run logic to condition a gate for clearing the run FF. The set output also satisfies gate U42 to satisfy gates U35 and U29. Gate U29 provides a not master clear plus reset signal to the address logic to clear the address register. A master clear and the scan signal from the select logic satisfies gate U41. The output of gate U41 also satisfies gates U35 and U29, clears the cancel request FF in the send logic, and clears the frame FF in the character decode logic. When the run FF in the run logic is cleared, the third frame and send BP FFs are cleared. When the START switch on the panel is pressed and a not WBT stop signal from the receiver is inactive, the ETX sent FF is cleared.

2-58. Block Parity Generator. The block parity generator builds a block parity character during a block and is selected as the fourth framing character. The transfer block parity generator logic (sh. 4) consists of the BP register U14, U15, U20, and U21 with associated gating logic. The register receives selected data from the data select logic. Gate U36 is disabled by the not clear block parity 1 signal from the character decode logic, the not block parity signal from the block control logic, and the not MUX 0 signal from the select logic. When these signals are inactive and $\overline{TT0}$ occurs, gate U36 is satisfied to clock the register. Each FF in the register that receives a logic 1 from the data select logic is then toggled. This occurs for each framing and text character of a message block. Gate U36 is disabled for control characters and disabled when the send BP FF in the block control logic is set. The BP character is then selected in the data select logic. The not clear block parity 1 signal from the character decode logic clears the register and disables gate U36. If the BP ERROR switch on the panel is set, an error is forced into the BP character by disabling gates U25. Block parity bit 1 is then inverted to cause a block parity error. This tests the AIU block parity check logic.

2-59. Character Counter. The character counter logic (sh. 7) consists of counters U82, U83, and U84 with associated gating logic. The position of the TRAN/REC switch determines if the count is to be incremented by an increment Tx or increment Rx signal. For each signal, the counter is clocked to display the current signal count on the panel.

2-60. Panel Control. The panel control logic consists of the CAN and REP FFs (sh. 3), step FF (sh. 5), and start FF (sh. 6). The panel control logic also includes the memory control write FF, load FFs, advance FFs, control FF (U62), and select FF (sh. 7). All the panel control FFs are set and cleared by operator switch action on the panel. The CAN and REP FFs are used to initiate send signals in the request control logic. The step FF controls the clock and timing for bit or character mode control. The start FF initiates the run logic after automatic operation is stopped. The write FF enables the RAM for a write operation. The load FFs load a memory address set in the ADDRESS switches into the address register. The advance FFs provide for sequential display of the selected memory. The control FF (U62) is set when any of the

memory control FFs are set. The output of the control FF presets the select FF in the select logic for the selected memory. The select FF selects the receiver memory data for display.

2-61. Figure 2-6 is a schematic diagram for the AIUTE panel. The signal names shown on this diagram correspond to signal names for switches and indicators referenced on the logic diagrams in figures 2-4 and 2-5. The AIUTE panel schematic diagram also supports the troubleshooting procedures in Chapter 3, Section IV, of this manual. Reference designations for the switch-indicator assembly numbers shown in figure 2-6 are identified in figure 2-7.

2-62. Figure 2-7 is an interconnection diagram for the AIUTE. The diagram shows interconnection cabling between assemblies and identifies the assembly numbers and reference designations.

D20003B_/19
(14243500B(01))

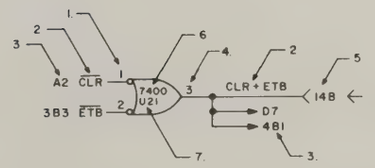
Receiver Section Logic Diagram
(Sheet 1 of 6)

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W.
2. UNLESS OTHERWISE SPECIFIED: CAPACITOR VALUES ARE IN MICROFARADS, ± 10%, 50V.
3. UNLESS OTHERWISE SPECIFIED: ALL CONNECTOR PINS ARE PREFIXED BY P1.
4. REFERENCE DRAWINGS:
   PWB: 14243400
   ASSY: 14243300

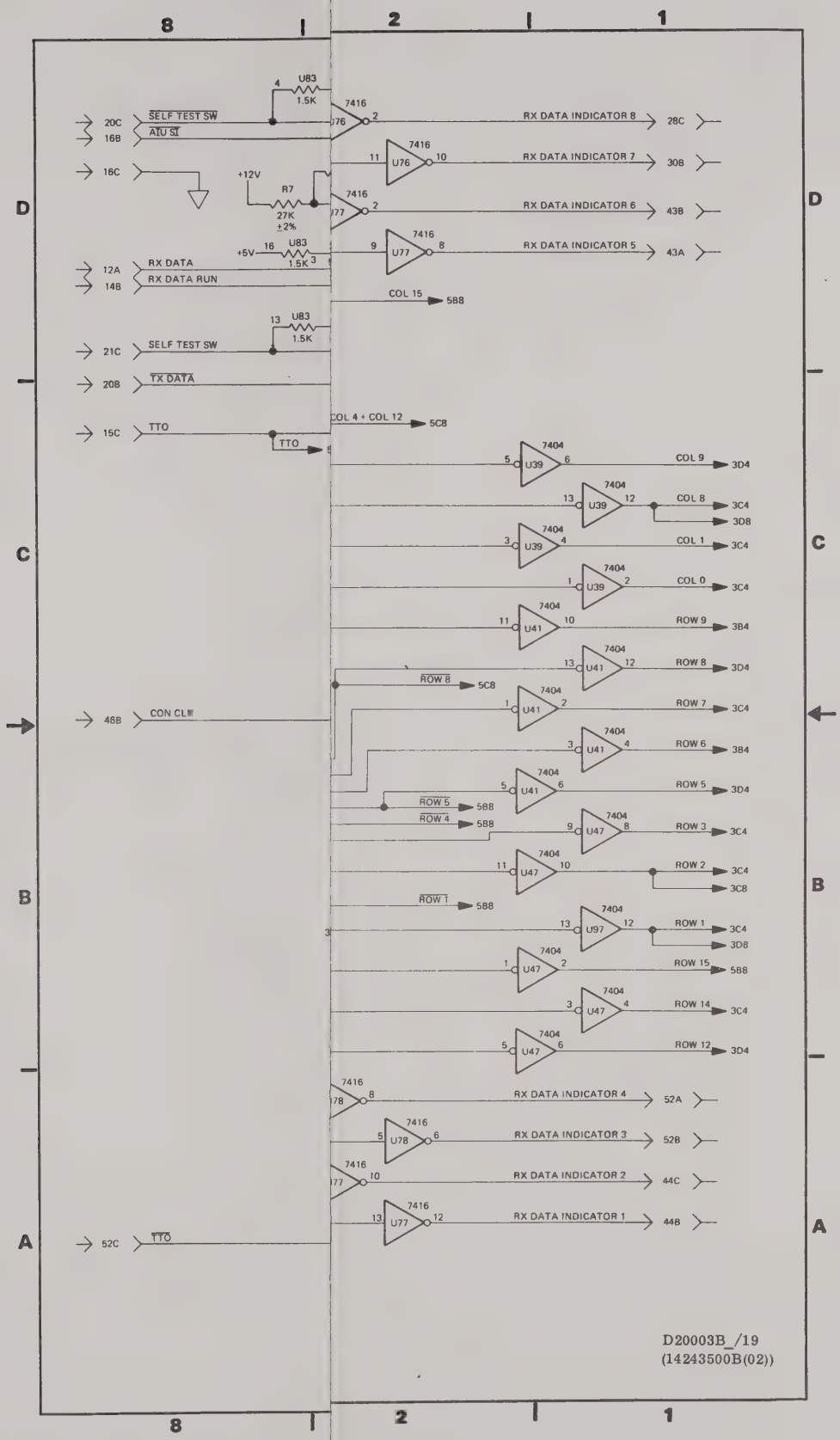
INPUT/OUTPUT SYMBOL INFORMATION

1. INPUT PIN NUMBERS
2. TERM NAME
3. DRAWING SHEET (IF DIFFERENT) AND ZONE OF TERM
4. OUTPUT PIN NUMBER
5. CONNECTOR SYMBOL AND PIN NUMBER
6. ELEMENT TYPE
7. INTEGRATED CIRCUIT LOCATION ON CIRCUIT CARD ASSEMBLY



D20003B_/19
(14243500B(01))

Figure 2-4. Receiver Section Logic Diagram (Sheet 1 of 6)



-4. Receiver Section Logic Diagram (Sheet 2 of 6)

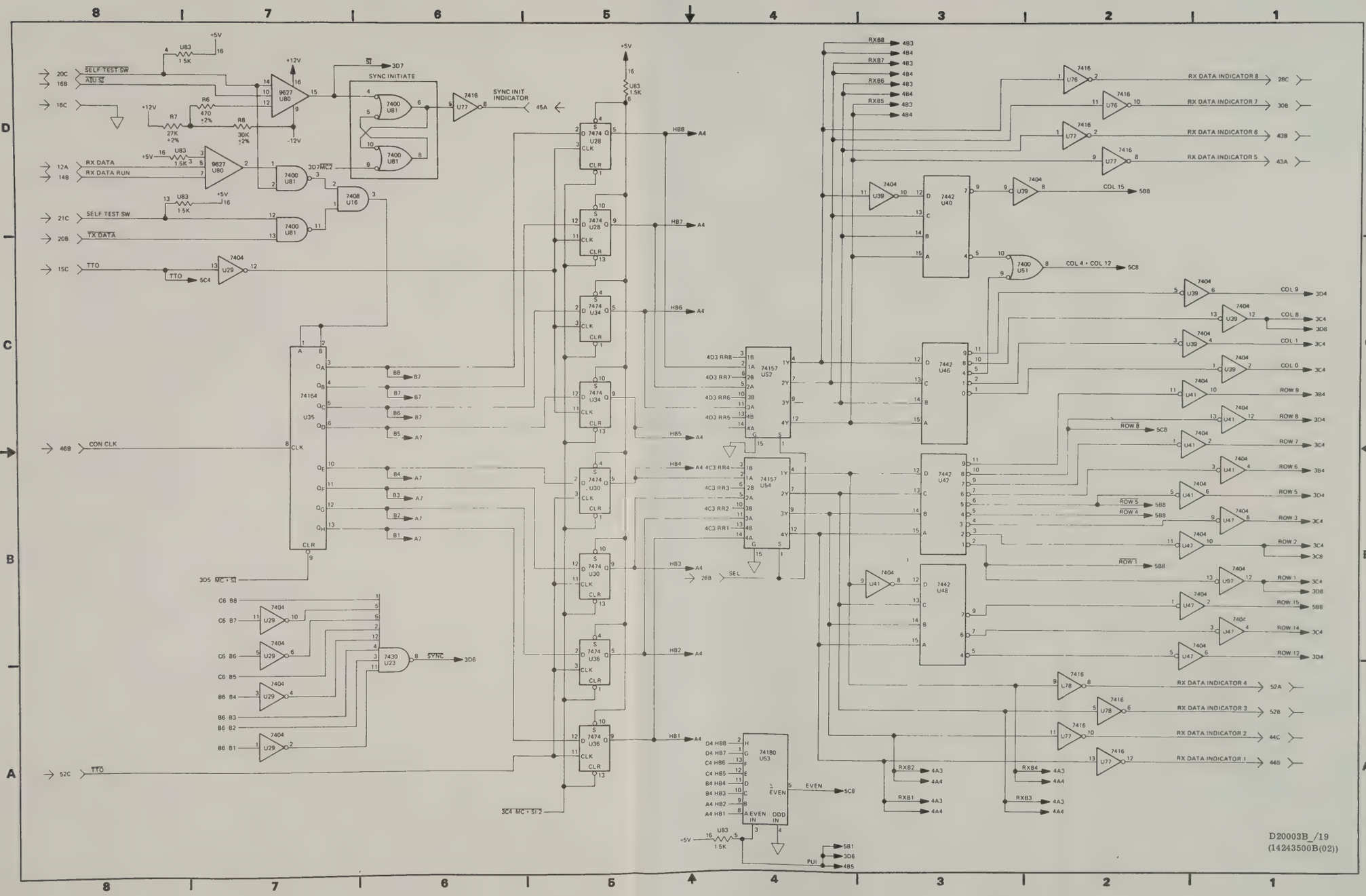
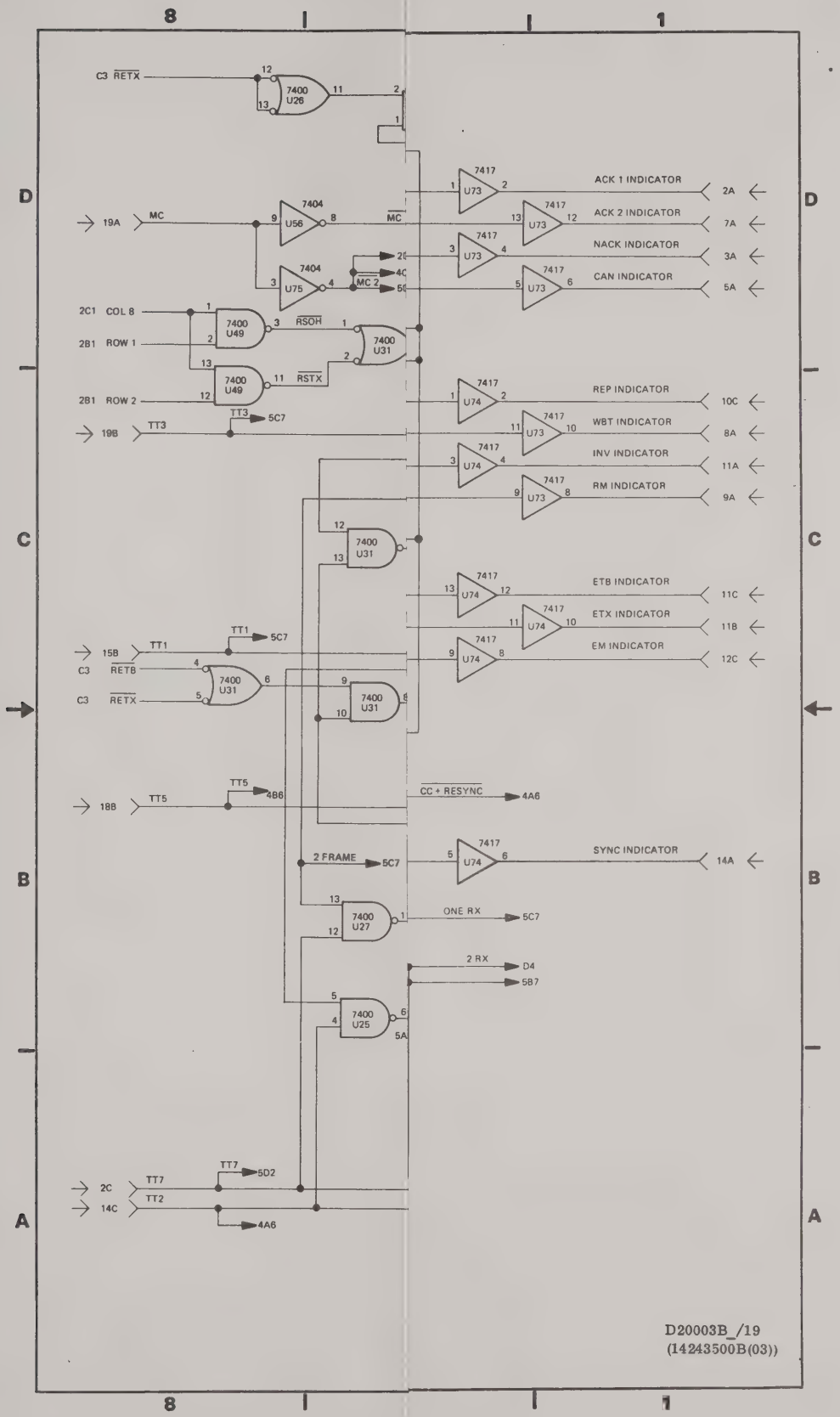


Figure 2-4. Receiver Section Logic Diagram (Sheet 2 of 6)



eceiver Section Logic Diagram
Sheet 3 of 6)

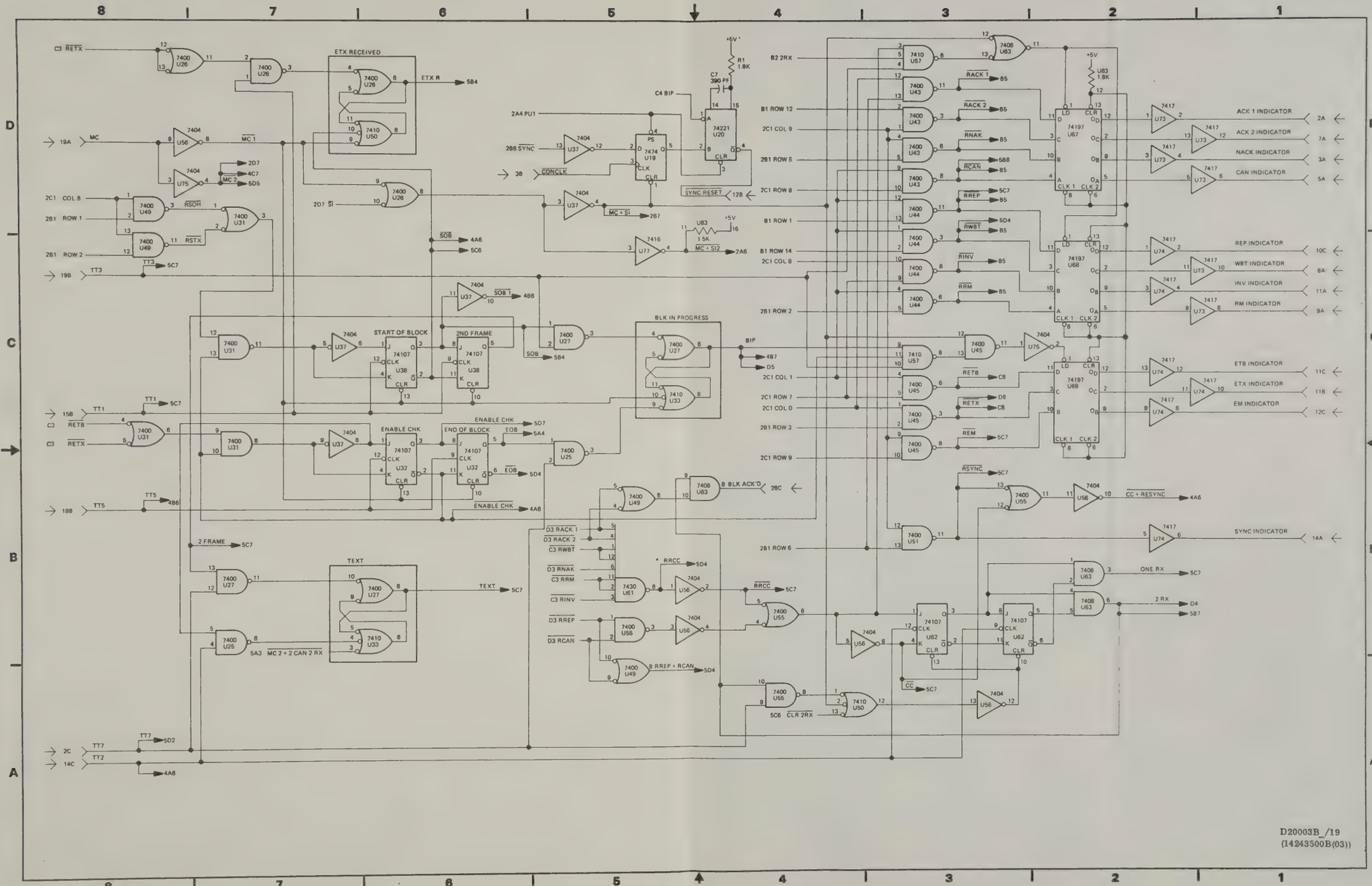
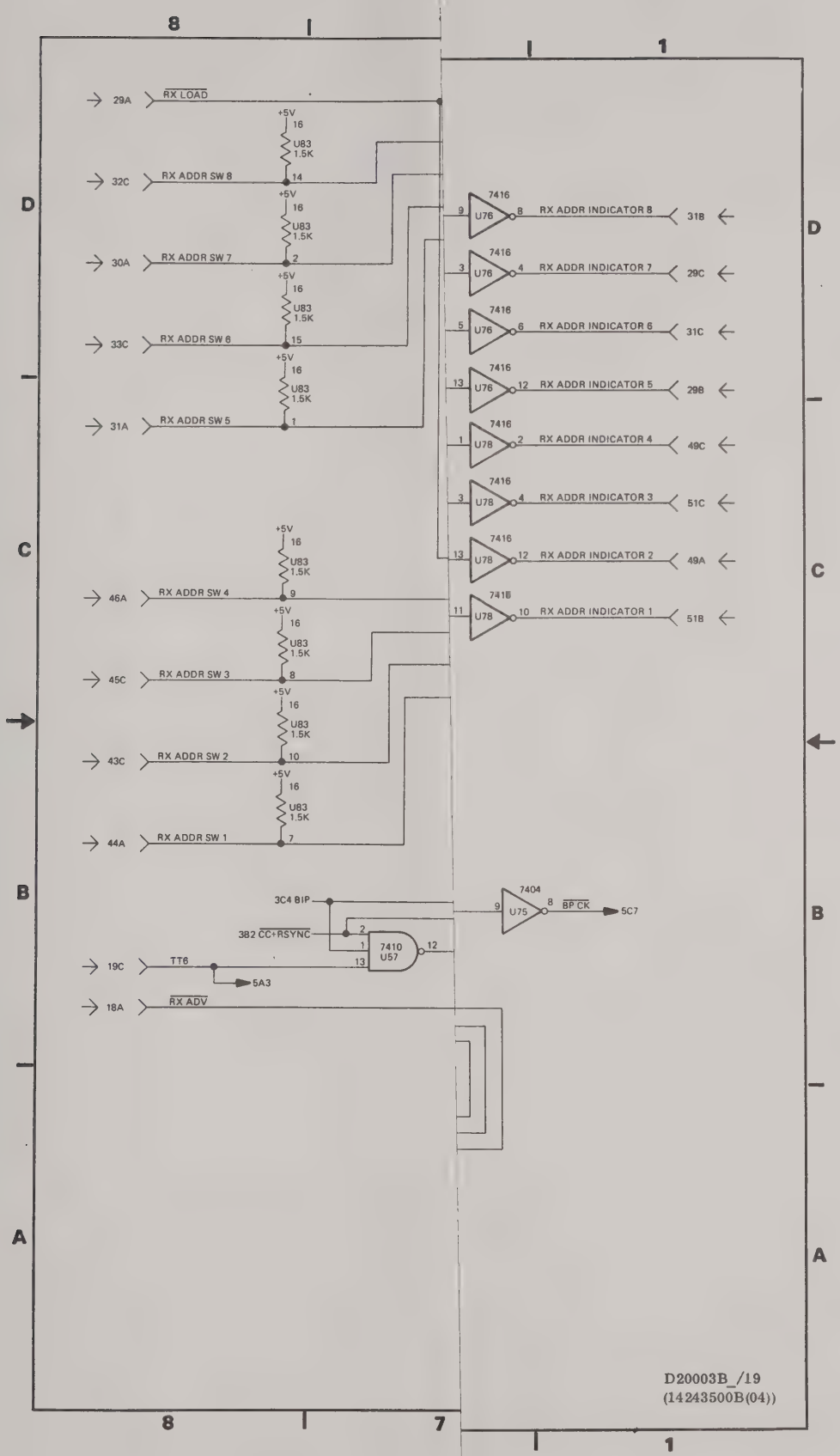


Figure 2-4. Receiver Section Logic Diagram (Sheet 3 of 6)



ver Section Logic Diagram
t 4 of 6)

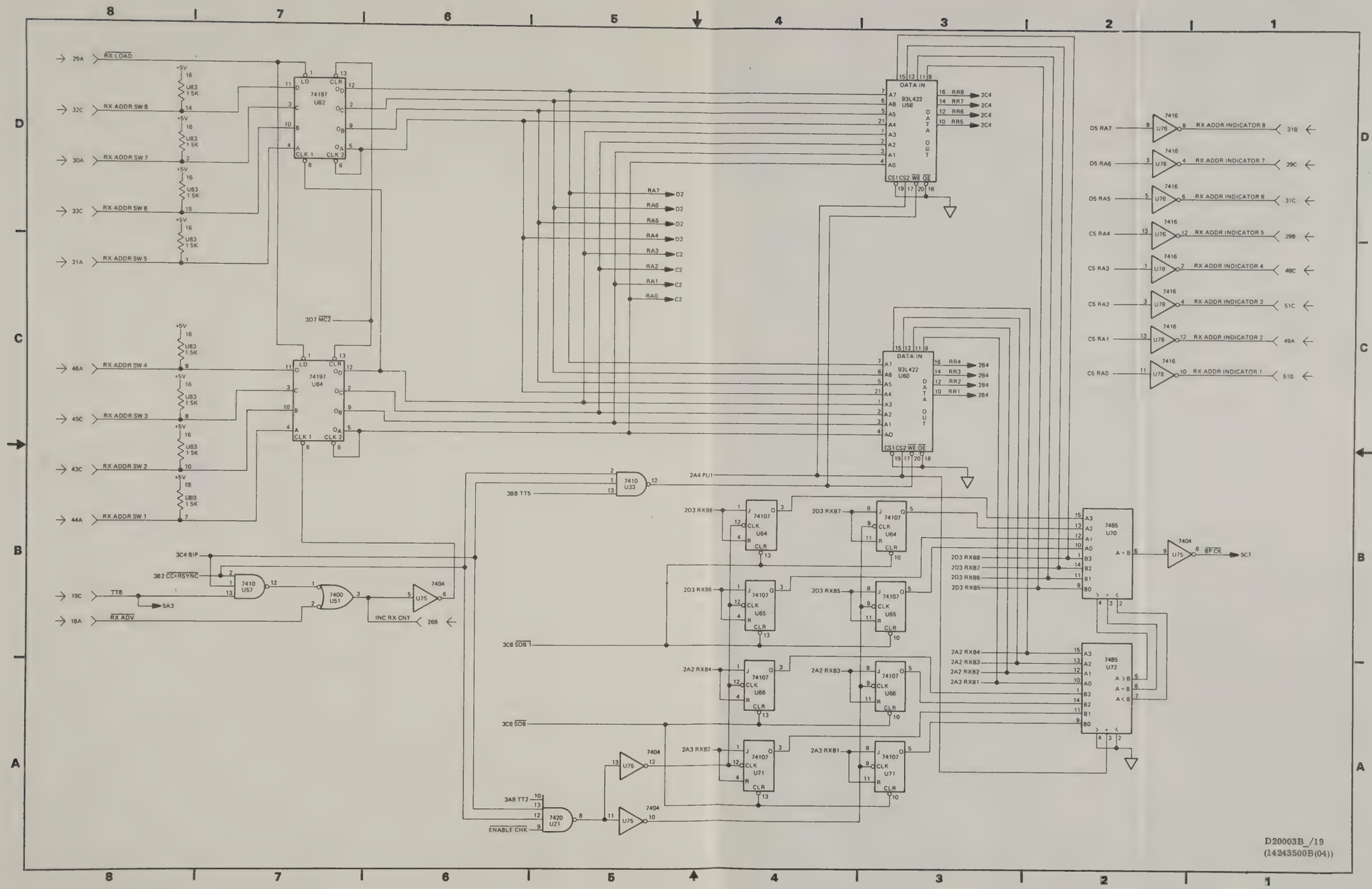
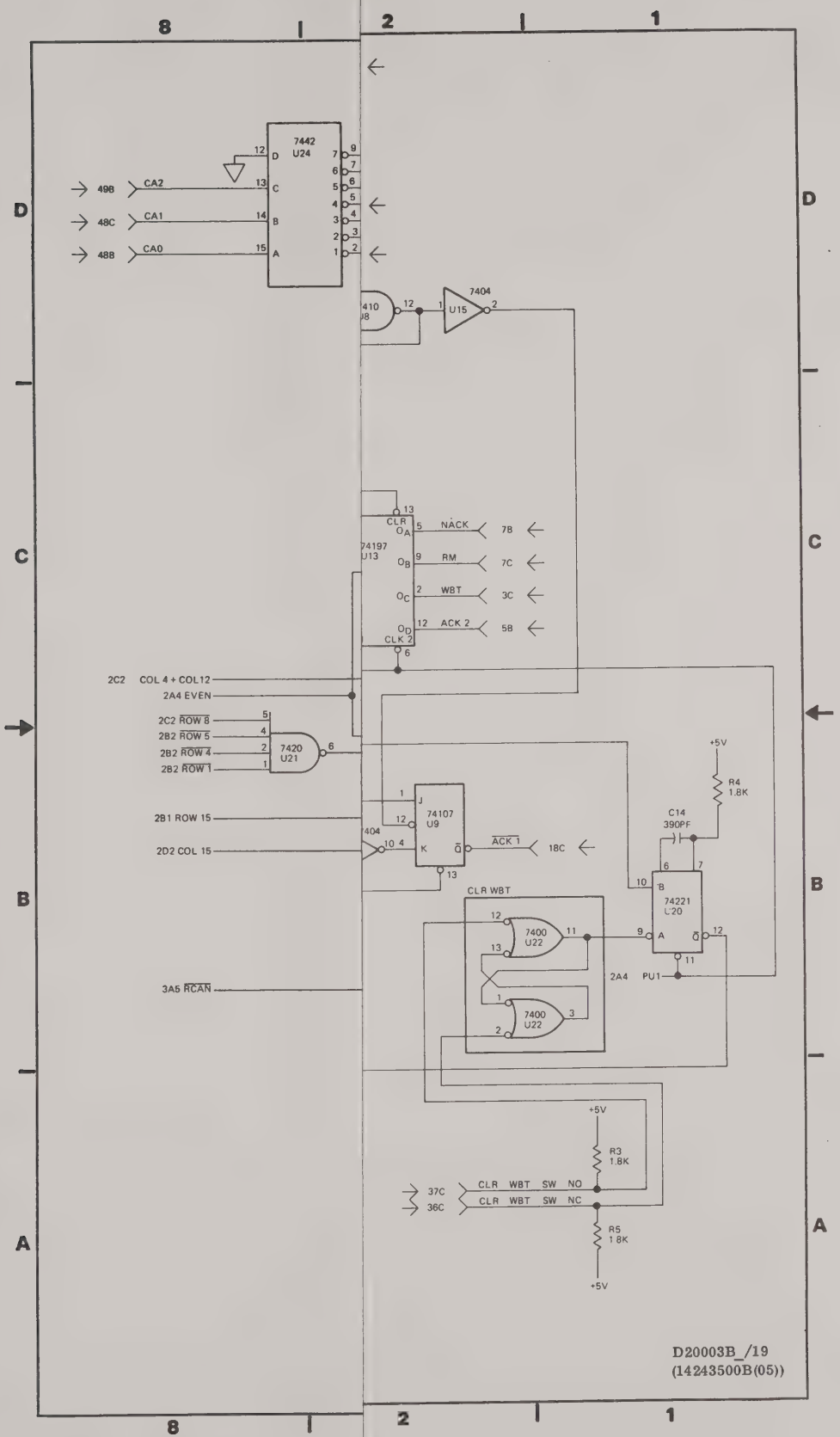


Figure 2-4. Receiver Section Logic Diagram
(Sheet 4 of 6)



Receiver Section Logic Diagram
(Sheet 5 of 6)

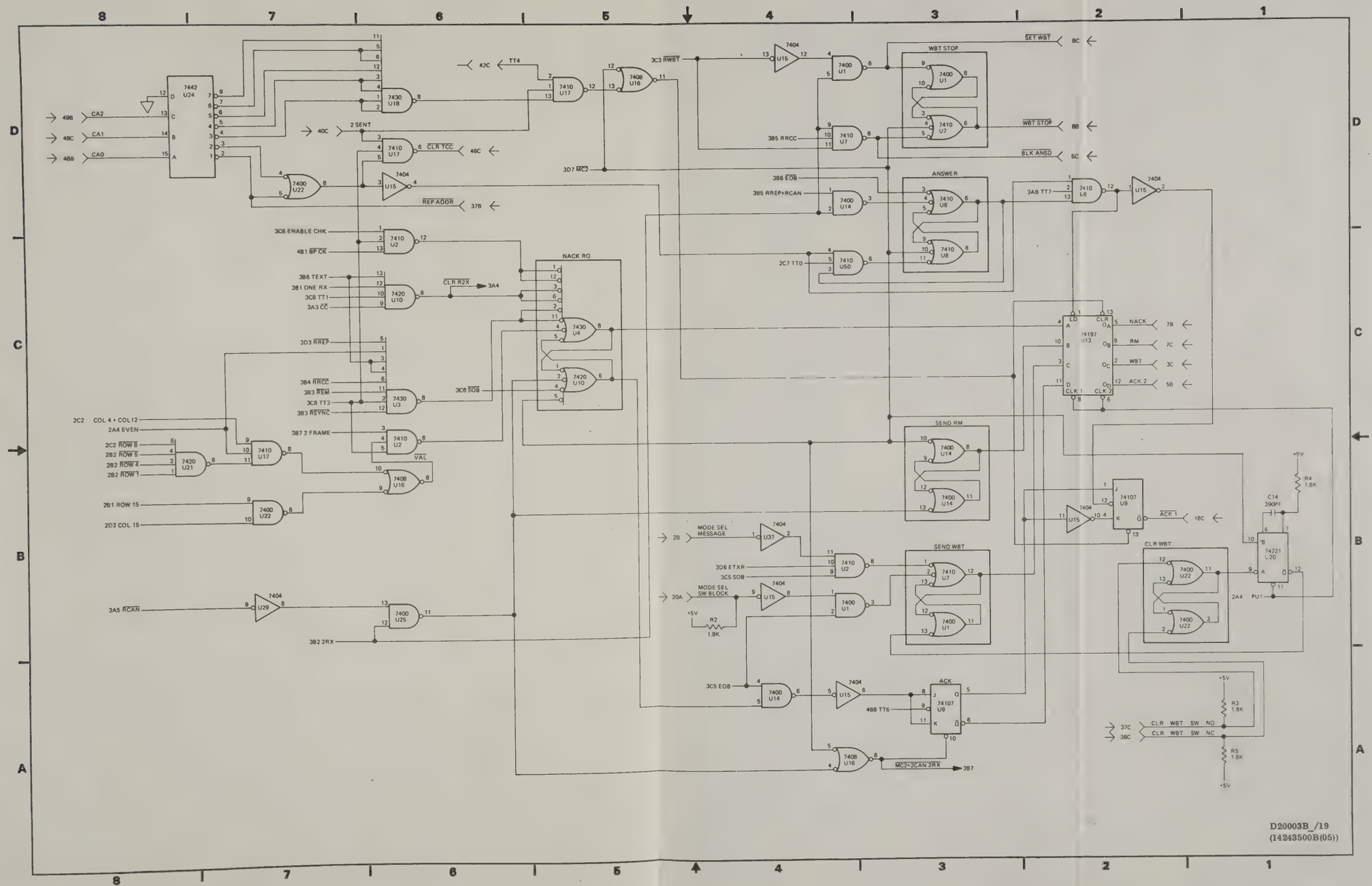


Figure 2-4. Receiver Section Logic Diagram (Sheet 5 of 6)

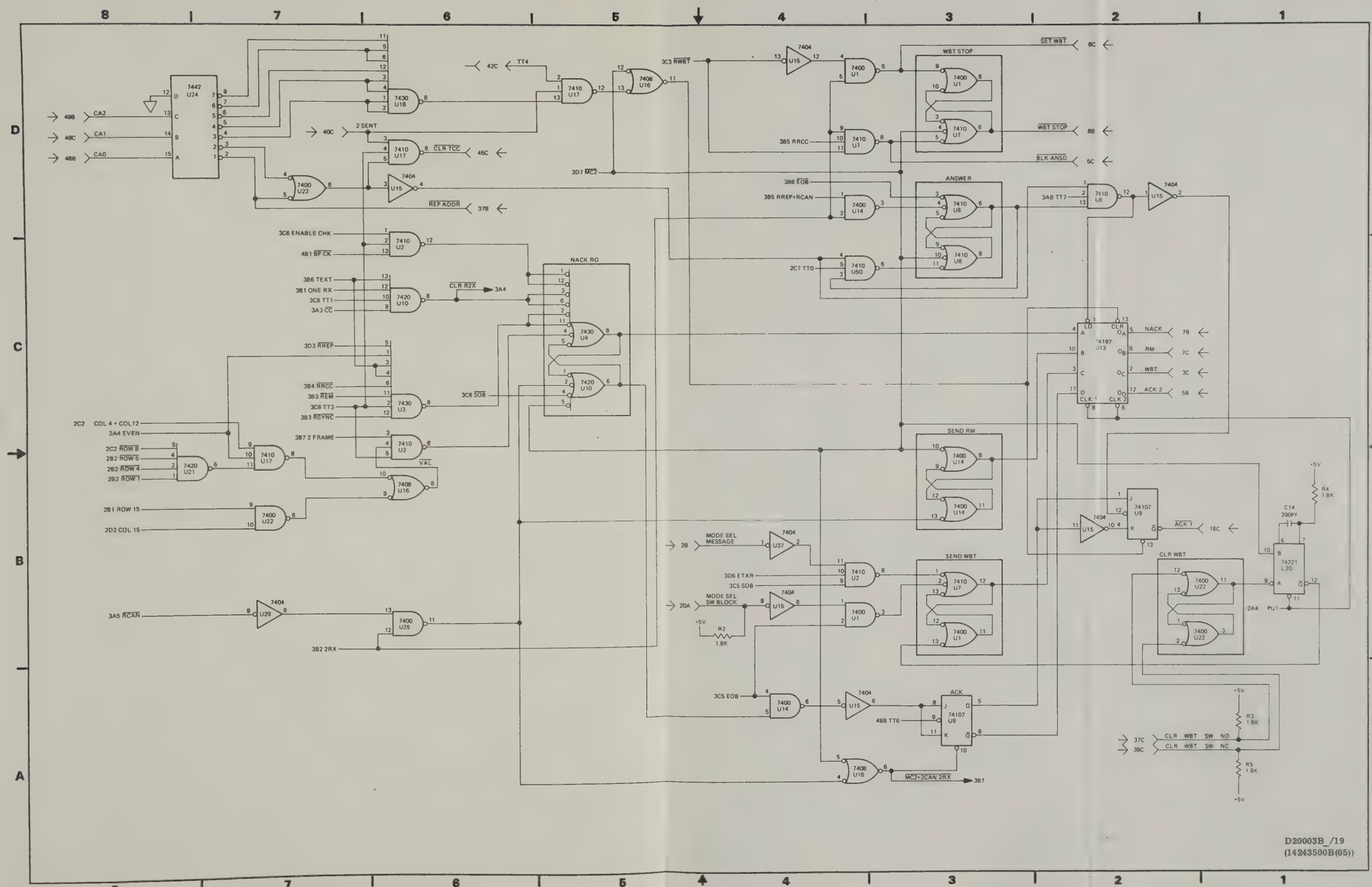
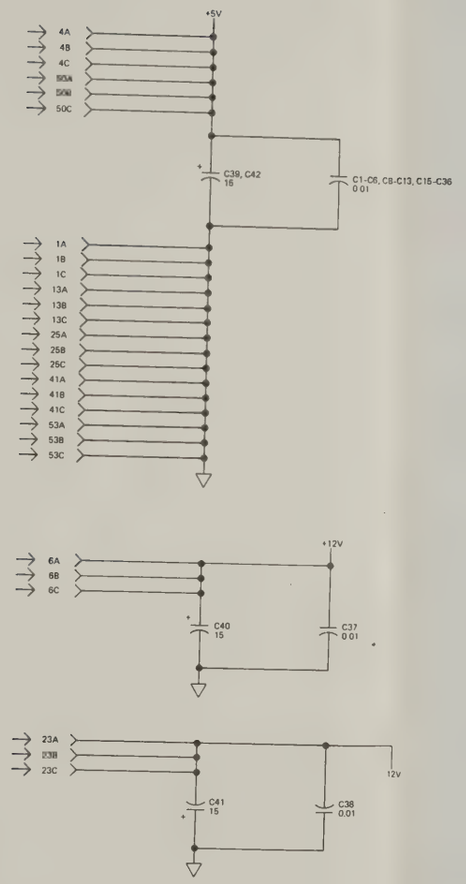
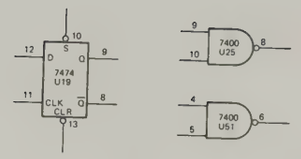


Figure 2-4. Receiver Section Logic Diagram (Sheet 5 of 6)

D20003B_/19
(14243500B(06))

Receiver Section Logic Diagram
(Sheet 6 of 6)





SPARE LOCATIONS

U5
U6
U11
U12

D20003B_/19
(14243500B(06))

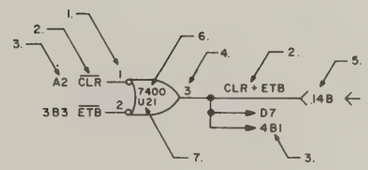
Figure 2-4. Receiver Section Logic Diagram (Sheet 6 of 6)

D20004B_/19
(14243200B(01))

r Section Logic Diagram
8)

INPUT/OUTPUT SYMBOL INFORMATION

1. INPUT PIN NUMBERS
2. TERM NAME
3. DRAWING SHEET (IF DIFFERENT) AND ZONE OF TERM
4. OUTPUT PIN NUMBER
5. CONNECTOR SYMBOL AND PIN NUMBER
6. ELEMENT TYPE
7. INTEGRATED CIRCUIT LOCATION ON CIRCUIT CARD ASSEMBLY

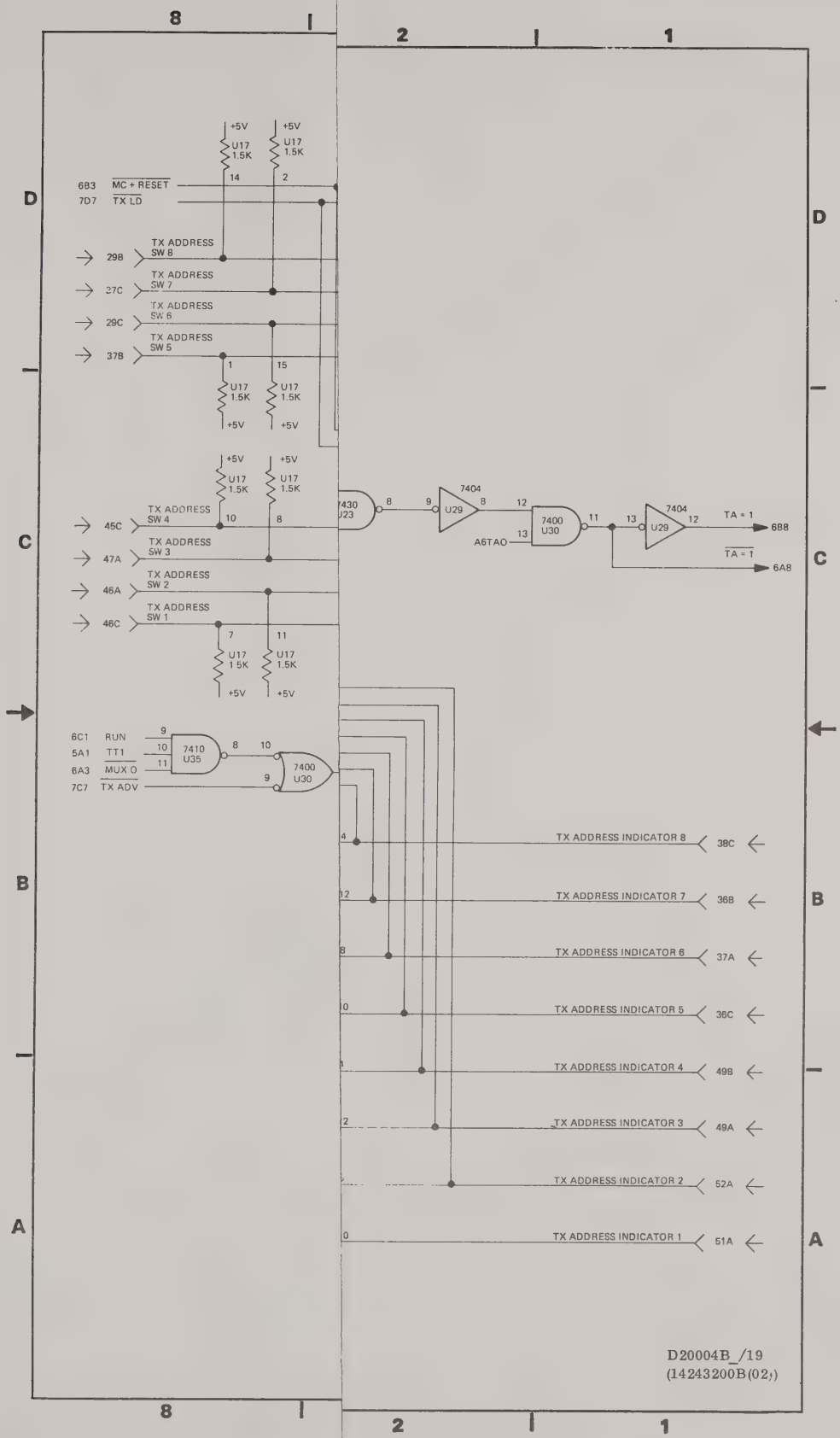


NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W.
2. UNLESS OTHERWISE SPECIFIED: CAPACITOR VALUES ARE IN MICROFARADS, ± 10%, 50V.
3. UNLESS OTHERWISE SPECIFIED: ALL CONNECTOR PINS ARE PREFIXED BY P1.
4. REFERENCE DRAWINGS:
   PWB: 14243100
   ASSY: 14243000

D20004B_/19
(14243200B(01))

Figure 2-5. Transmitter Section Logic Diagram (Sheet 1 of 8)



Transmitter Section Logic Diagram
(Sheet 2 of 8)

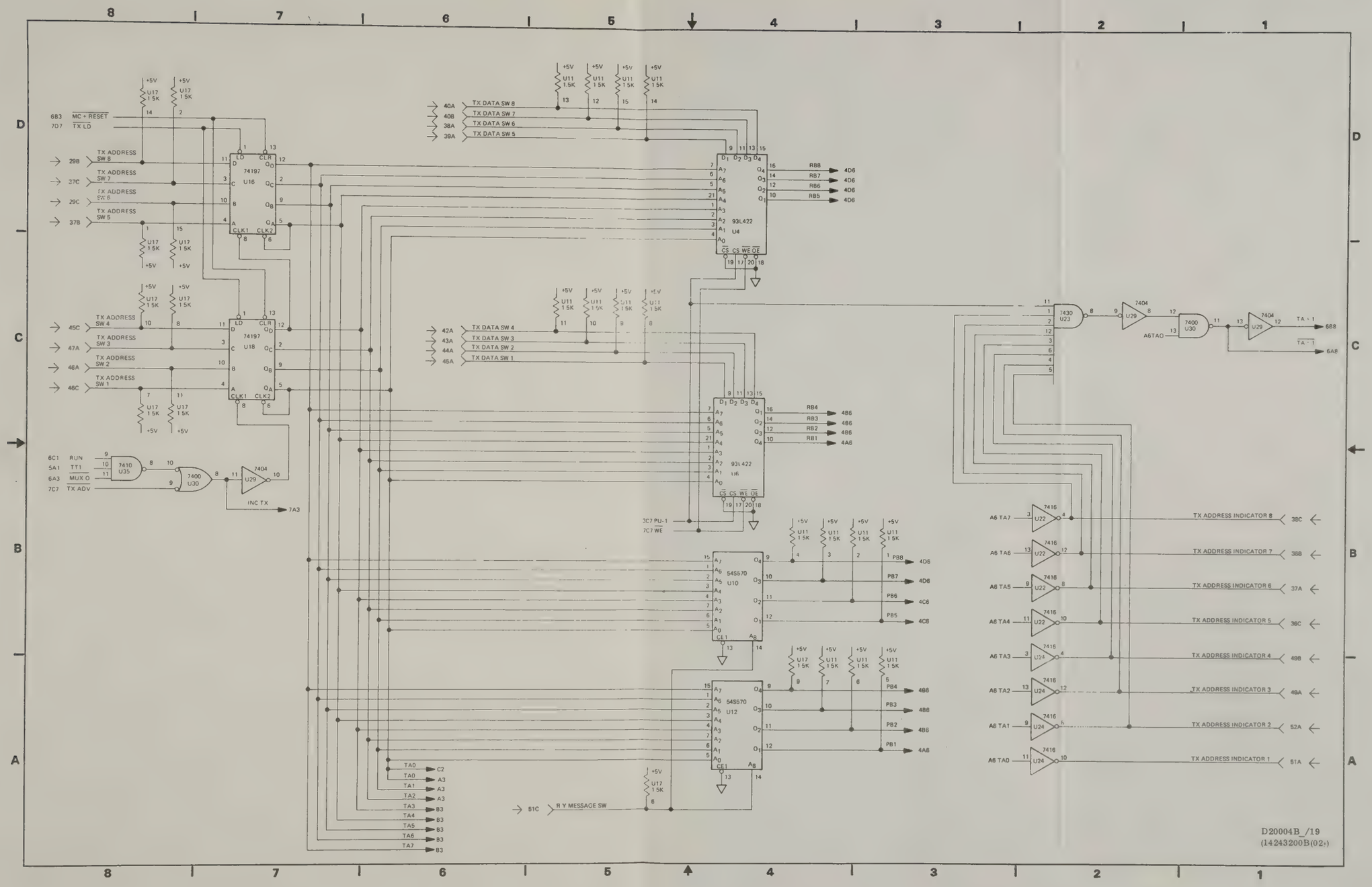
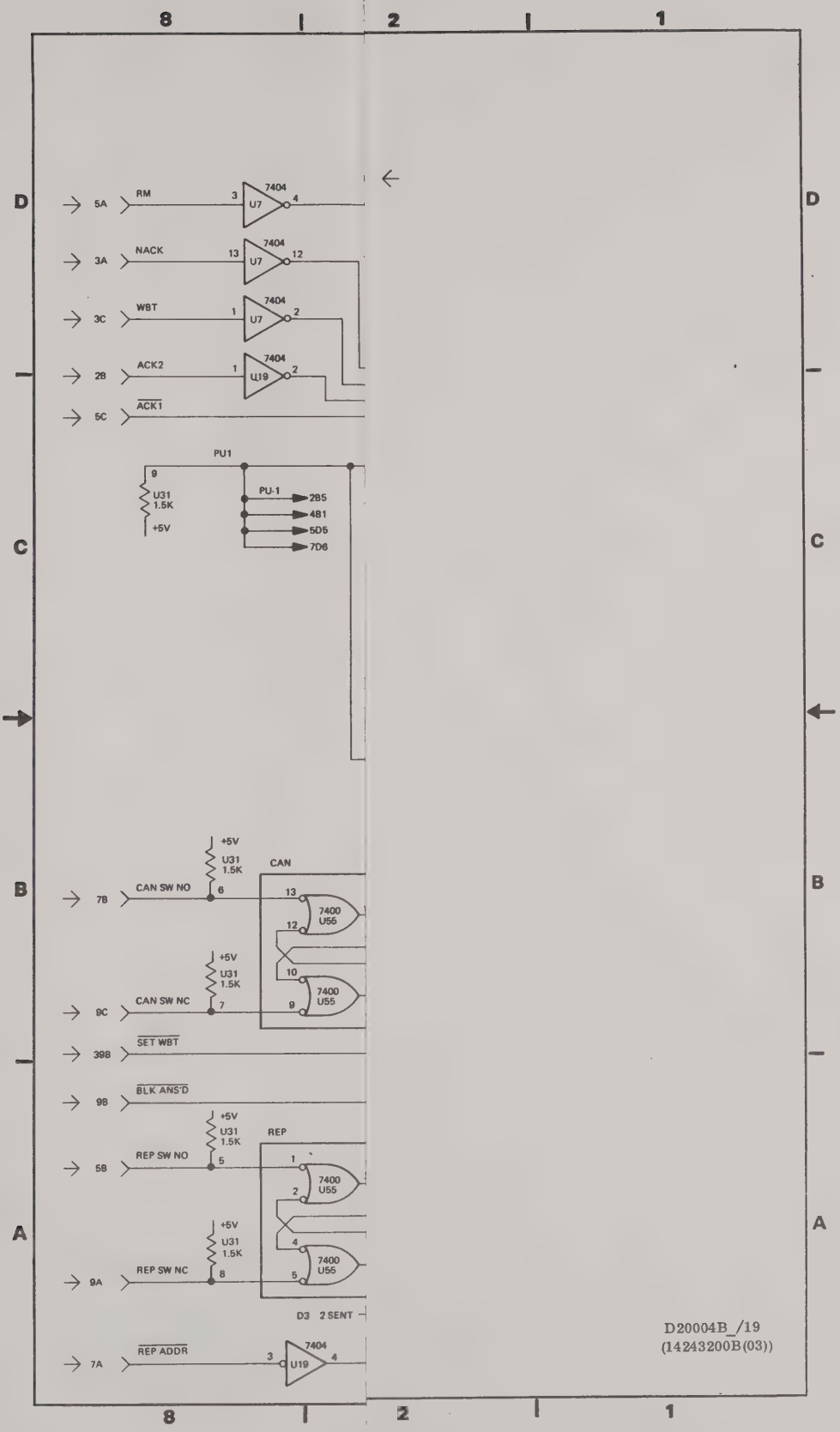


Figure 2-5. Transmitter Section Logic Diagram (Sheet 2 of 8)



Transmitter Section Logic Diagram
(Sheet 3 of 8)

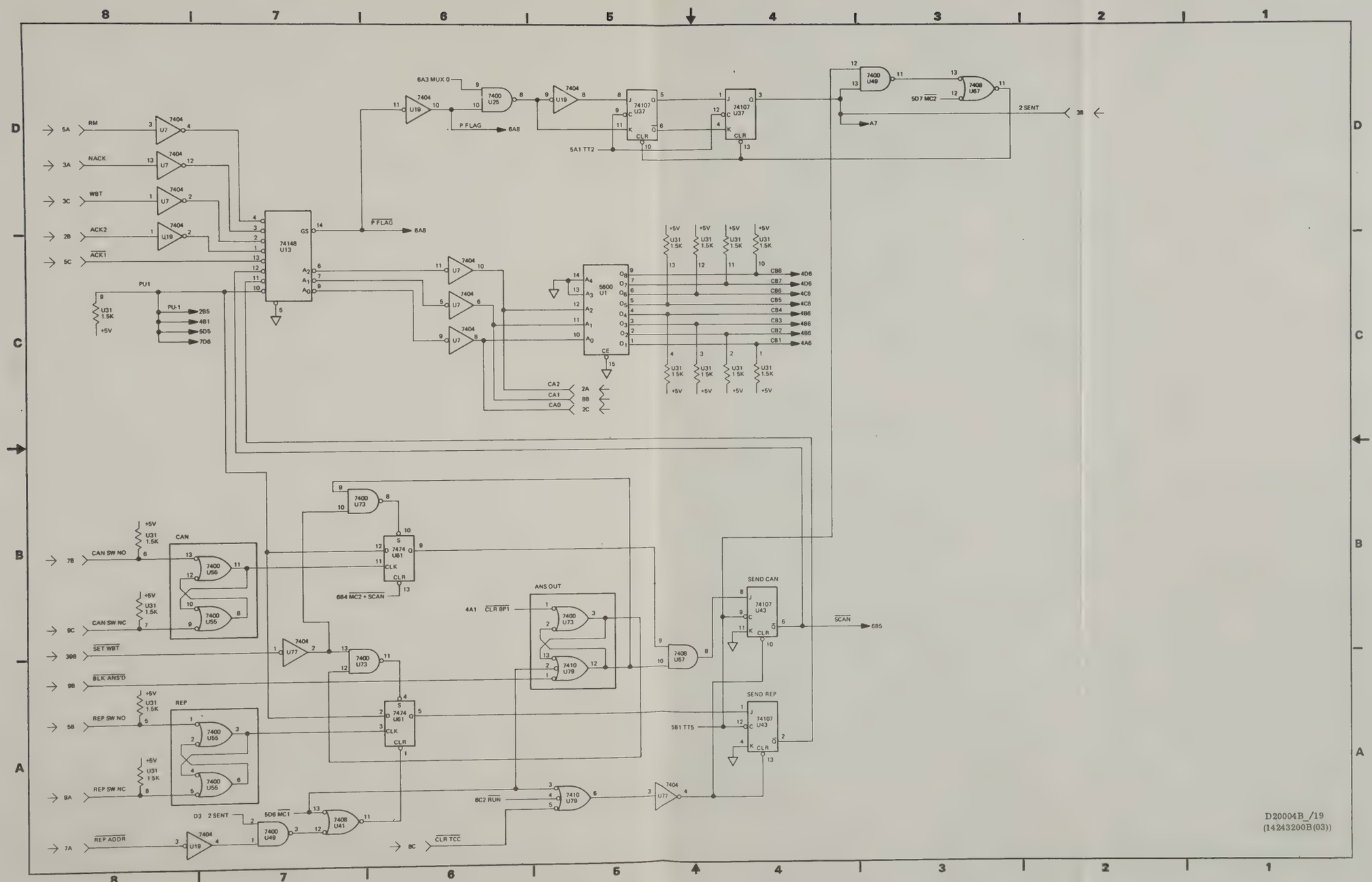
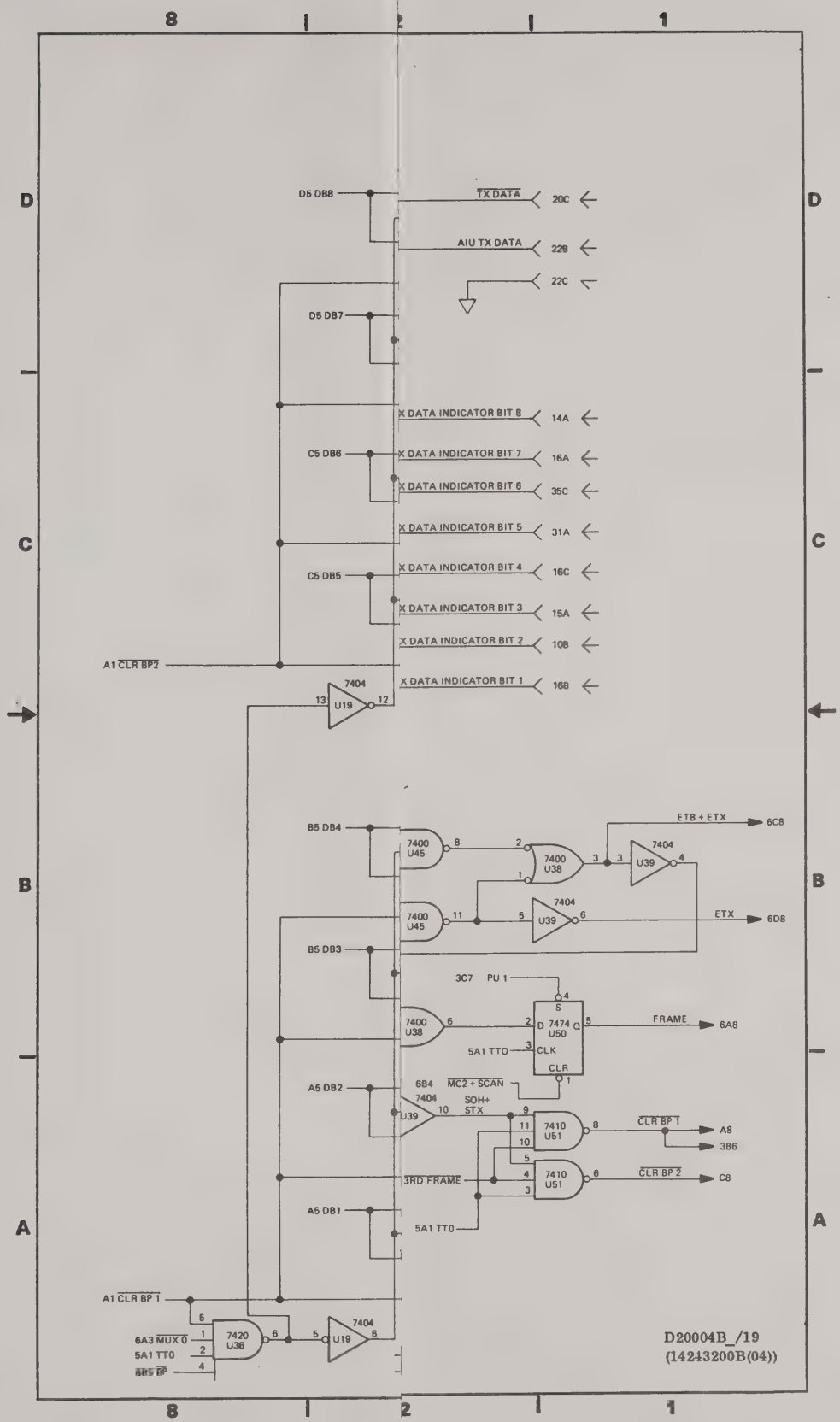


Figure 2-5. Transmitter Section Logic Diagram (Sheet 3 of 8)



nsmitter Section Logic Diagram
et 4 of 8)

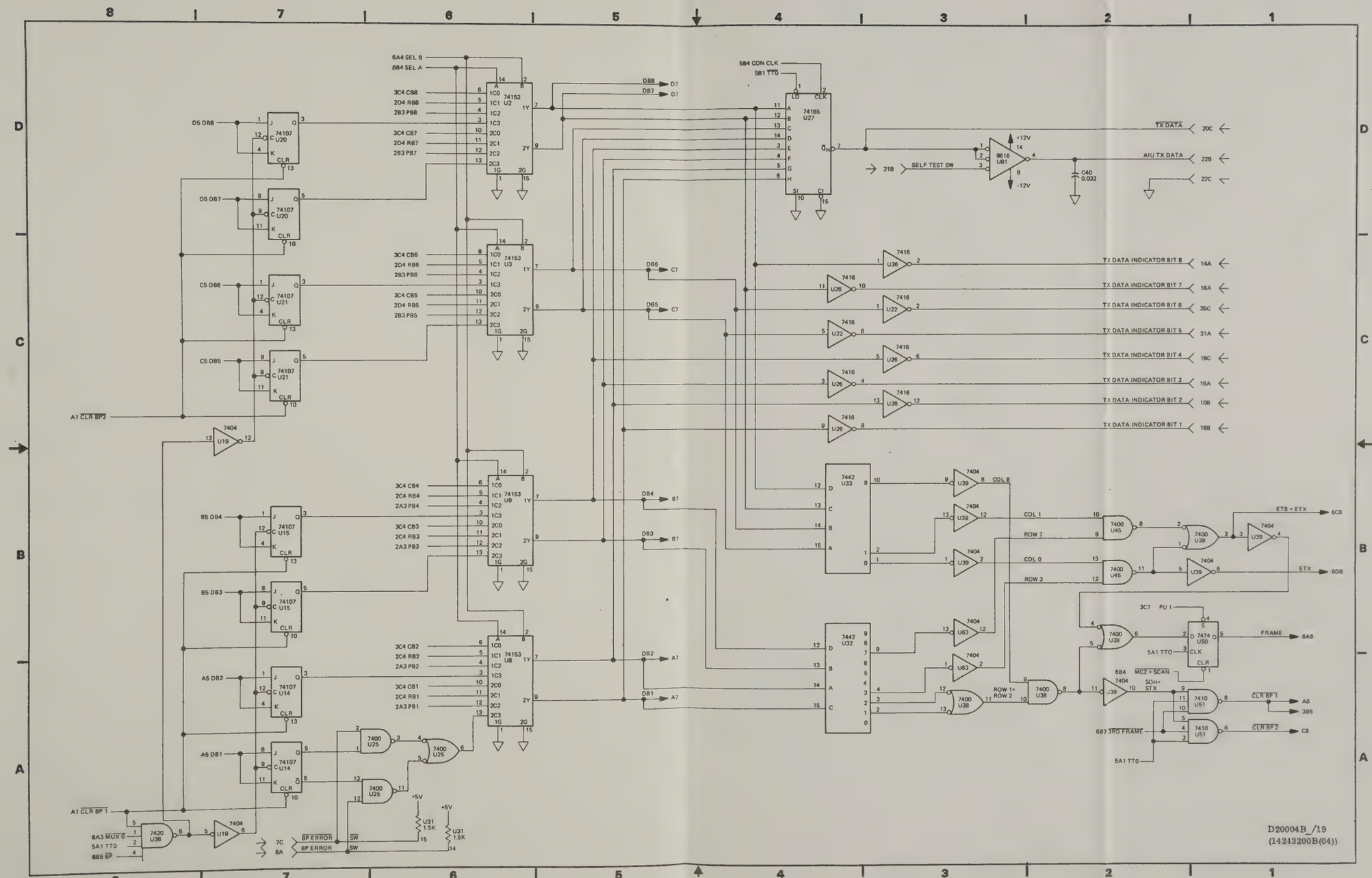
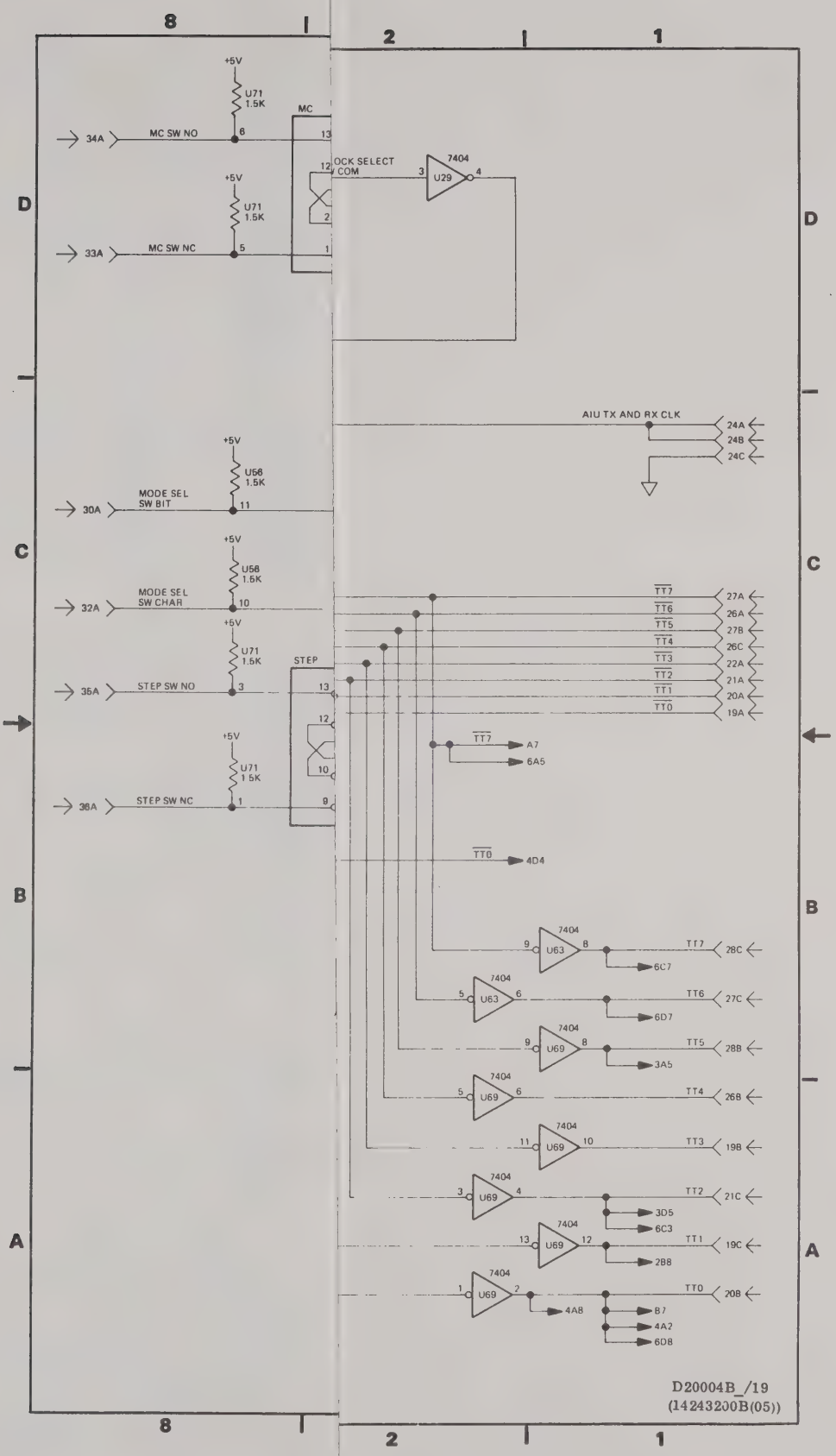


Figure 2-5. Transmitter Section Logic Diagram (Sheet 4 of 8)



Transmitter Section Logic Diagram
(Sheet 5 of 8)

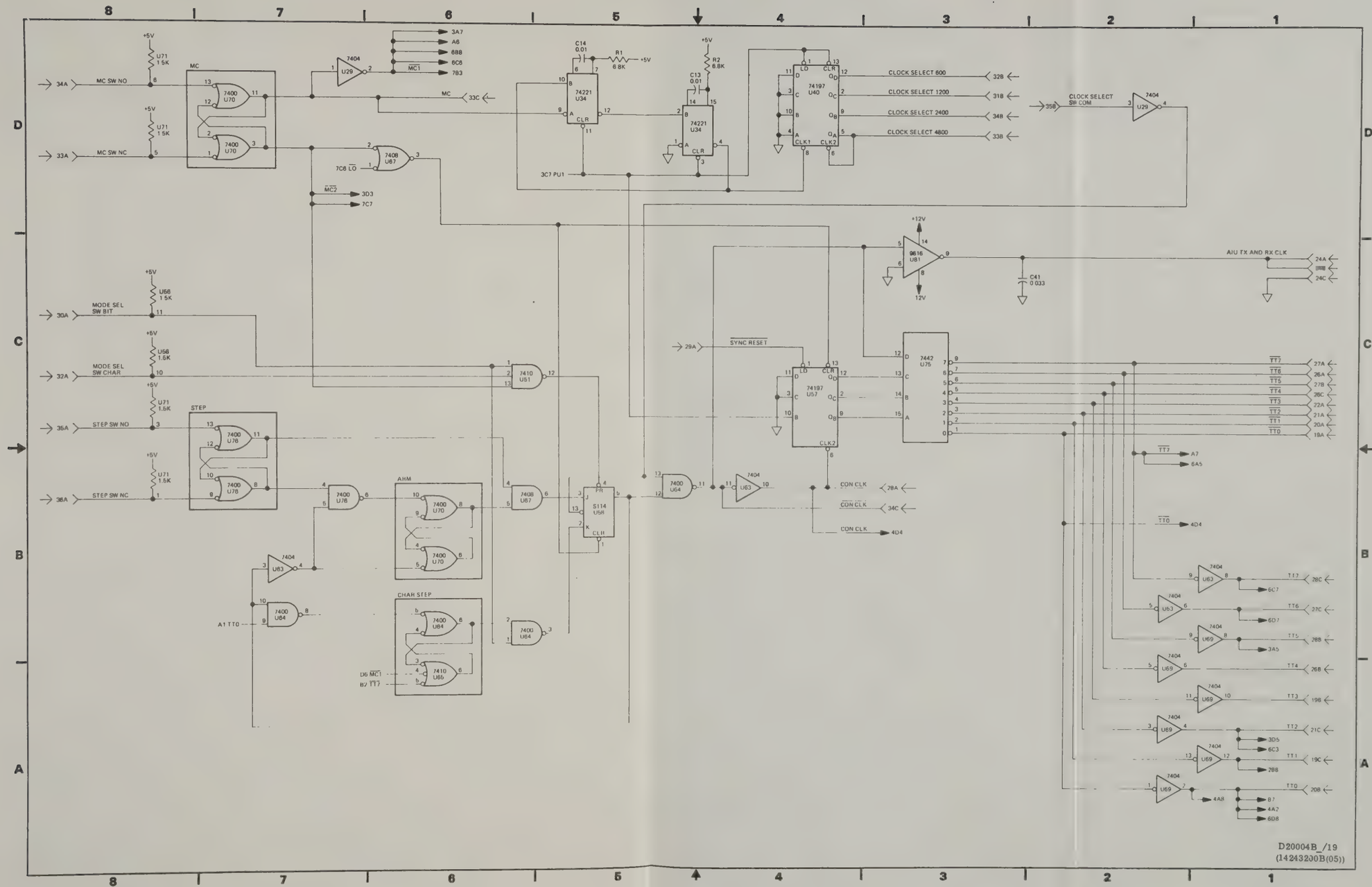
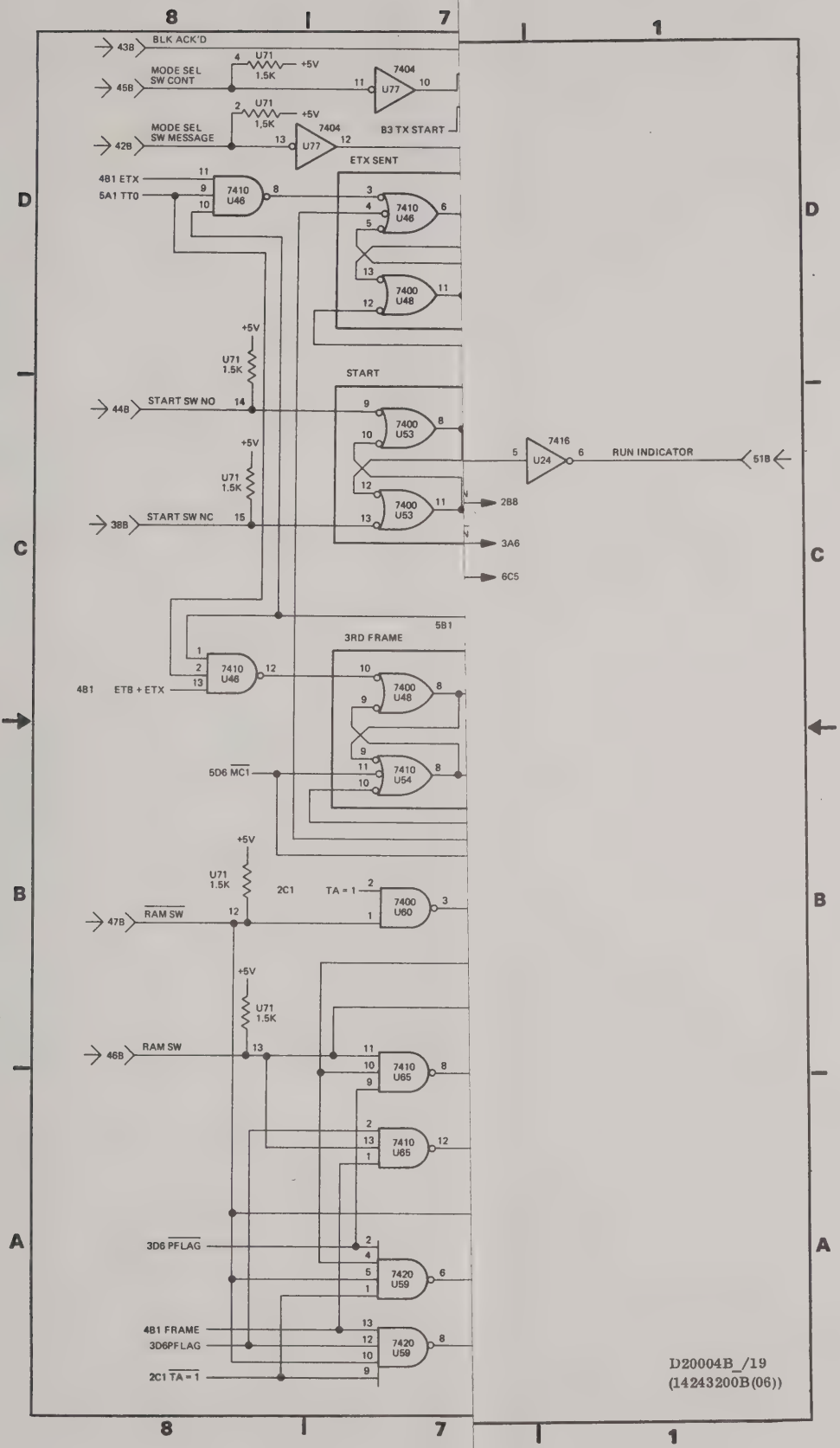


Figure 2-5. Transmitter Section Logic Diagram (Sheet 5 of 8)



ter Section Logic Diagram
of 8)

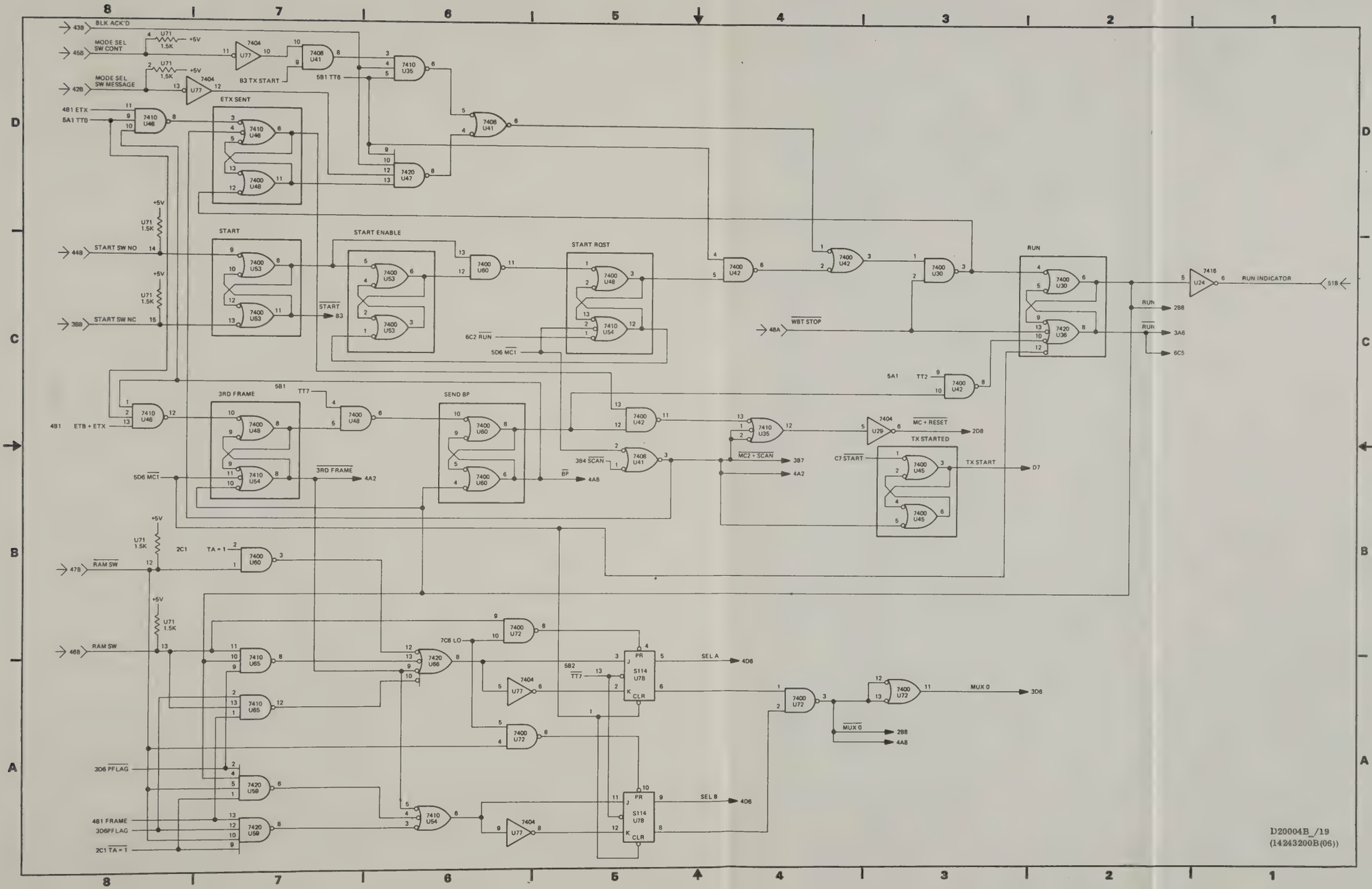
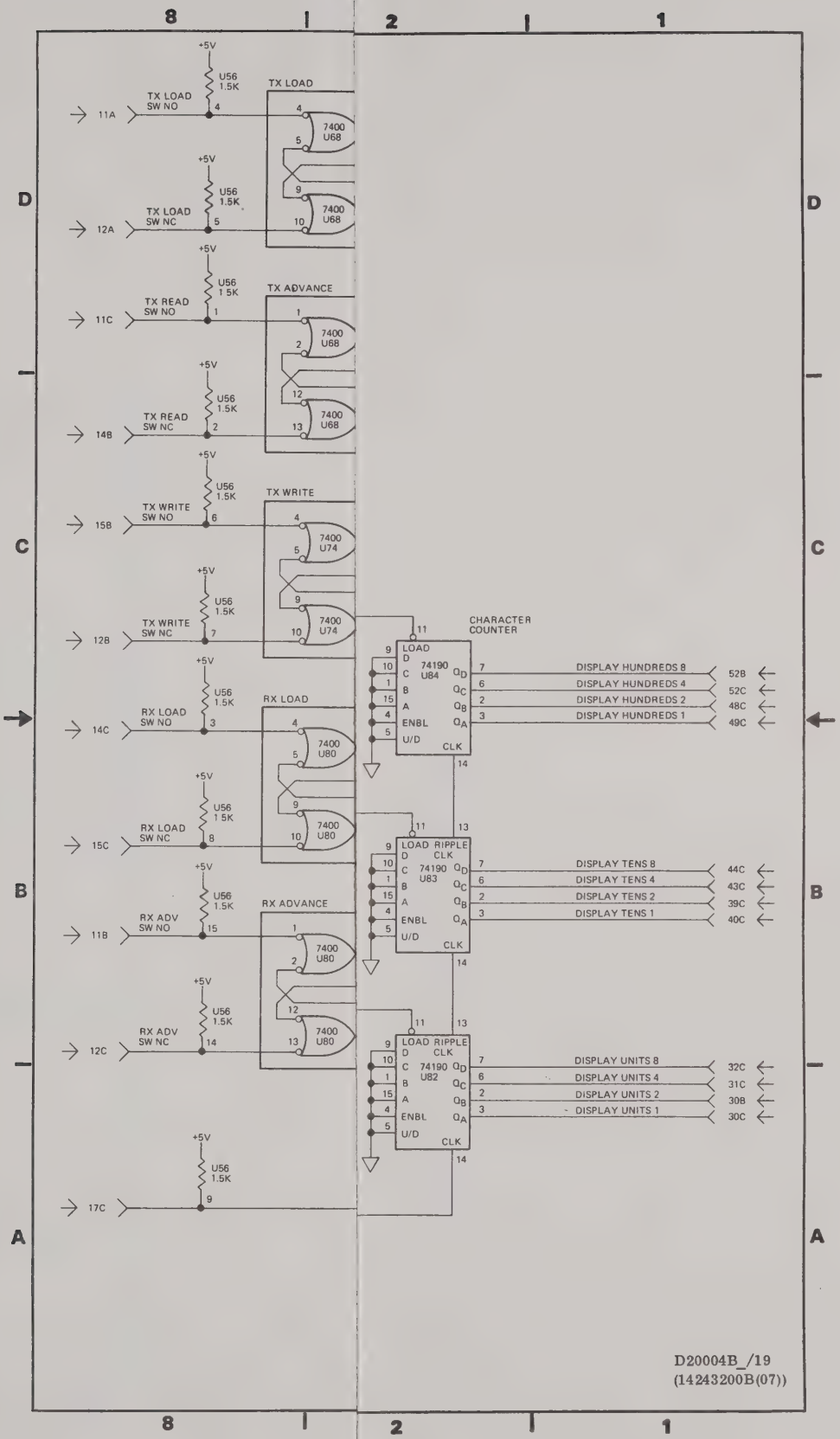


Figure 2-5. Transmitter Section Logic Diagram (Sheet 6 of 8)



Transmitter Section Logic Diagram
(Sheet 7 of 8)

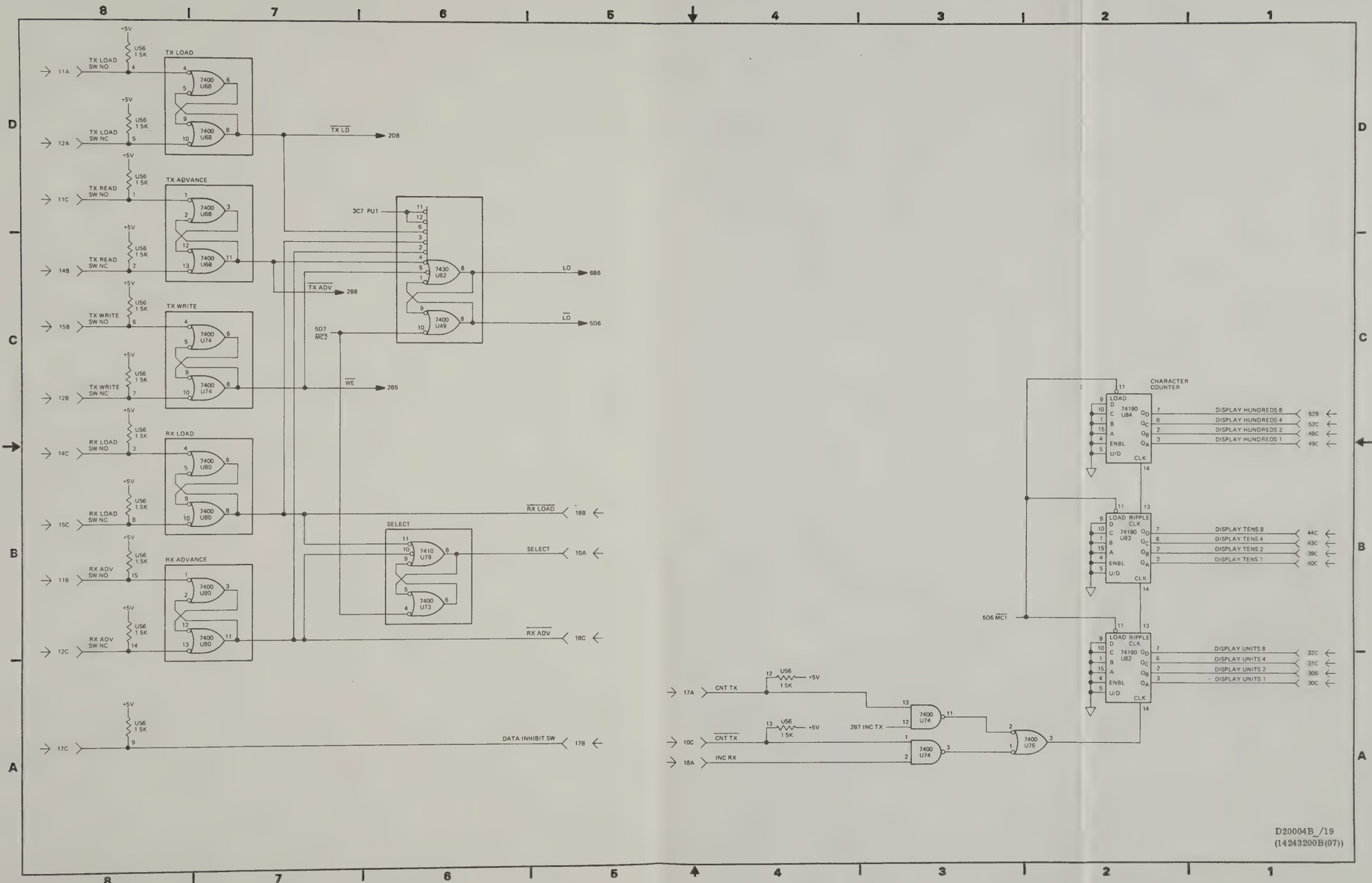
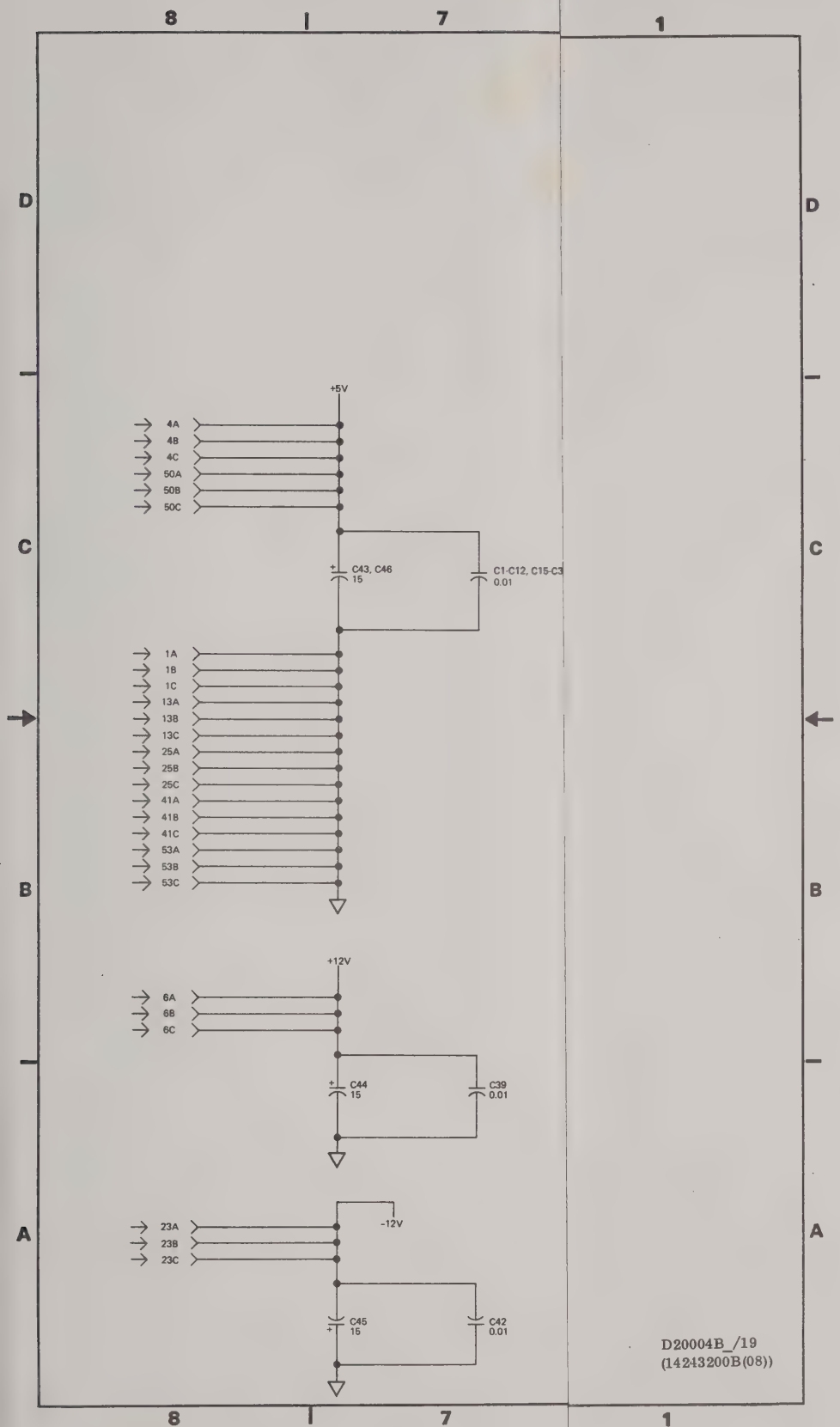


Figure 2-5. Transmitter Section Logic Diagram (Sheet 7 of 8)



ion Logic Diagram

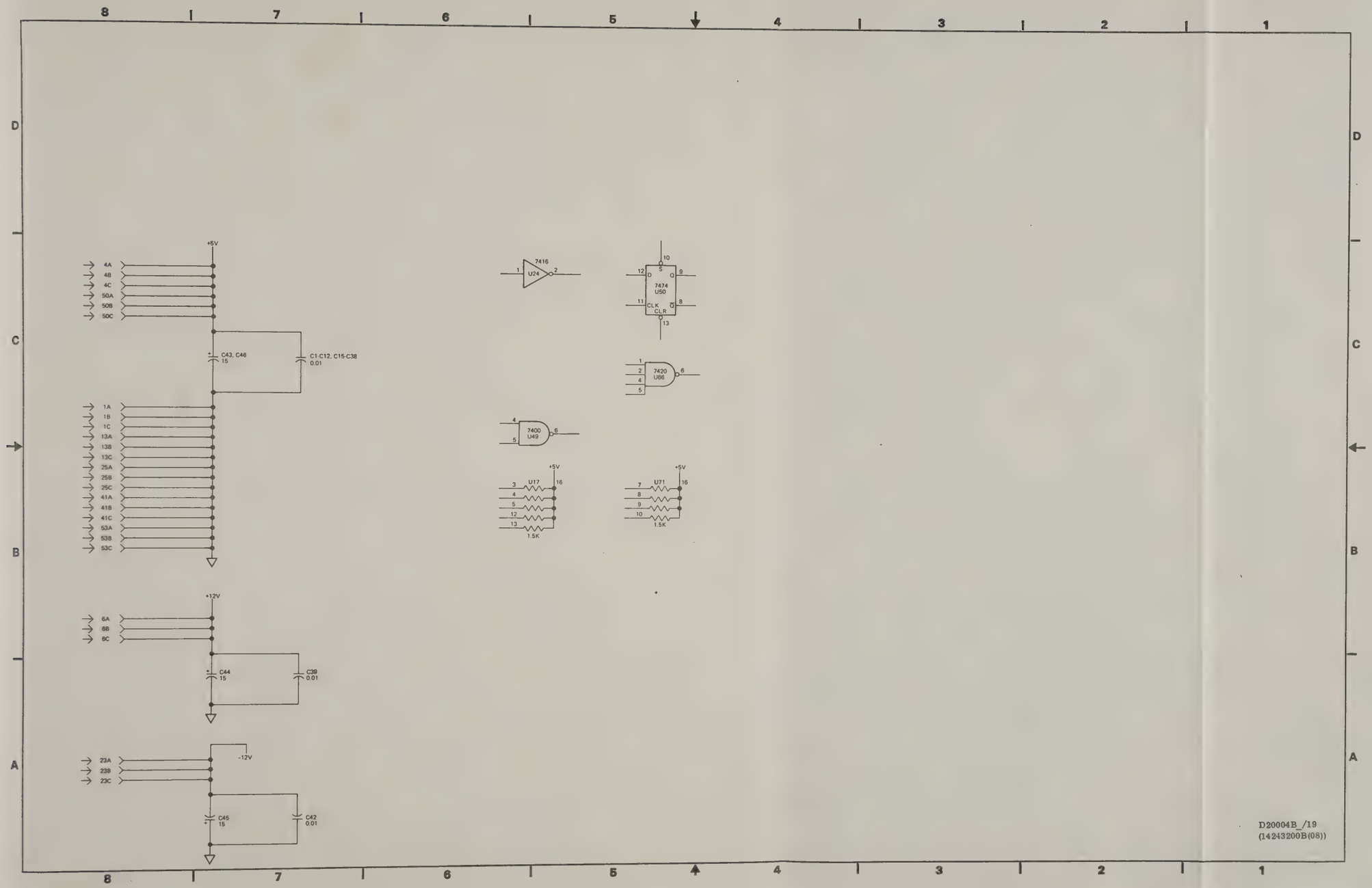


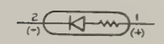
Figure 2-5. Transmitter Section Logic Diagram (Sheet 8 of 8)

D20005B_/19
(14394700B(01))

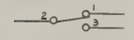
TE Panel Schematic Diagram
et 1 of 3)

TYPICAL PIN NUMBERS
FOR

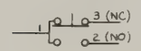
LED INDICATOR



TOGGLE SWITCH



PUSH BUTTON SWITCH

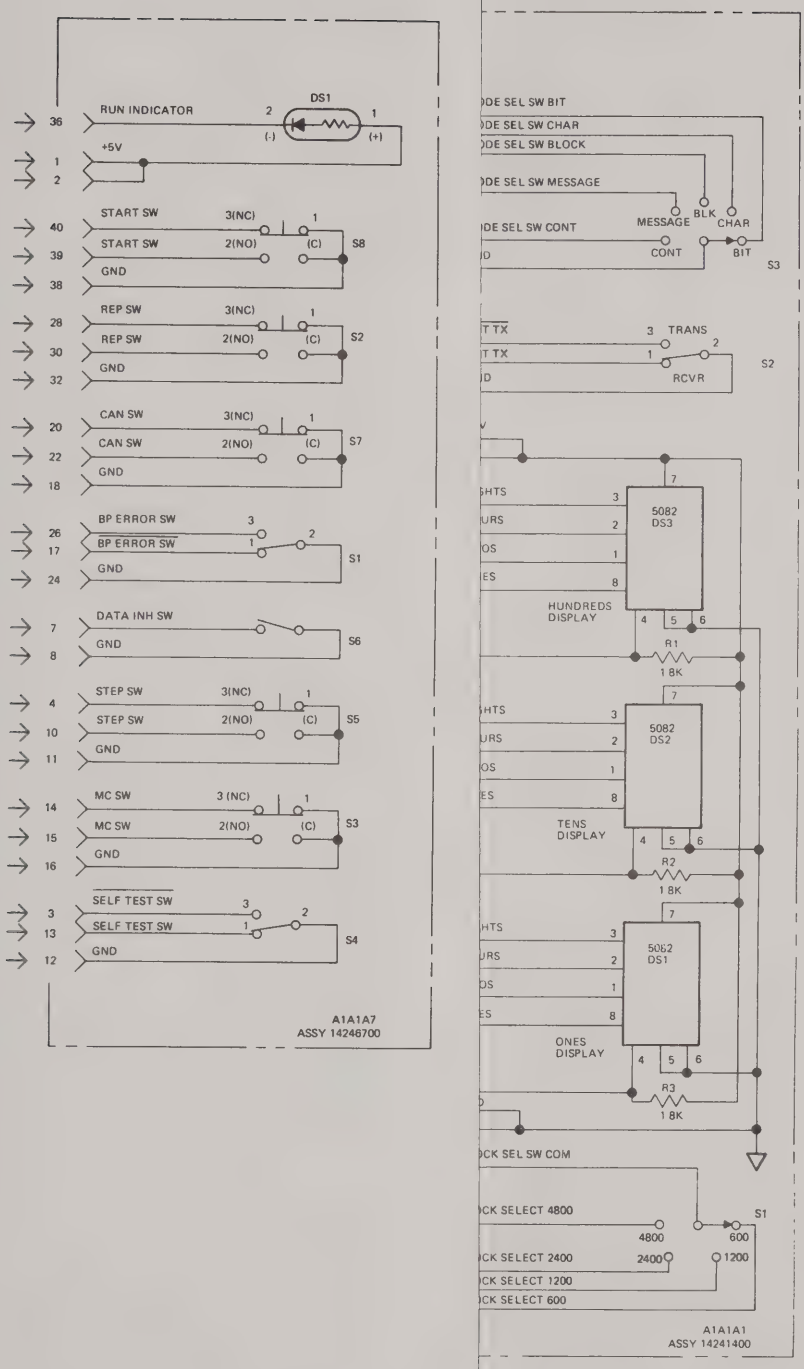


NOTES:

1. GRAPHIC SYMBOLS PORTRAYED CONFORMS TO ANSI Y32.2.
2. UNLESS OTHERWISE SPECIFIED: RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W.
3. UNLESS OTHERWISE SPECIFIED: ALL CONNECTOR PINS ARE PREFIXED BY J1.

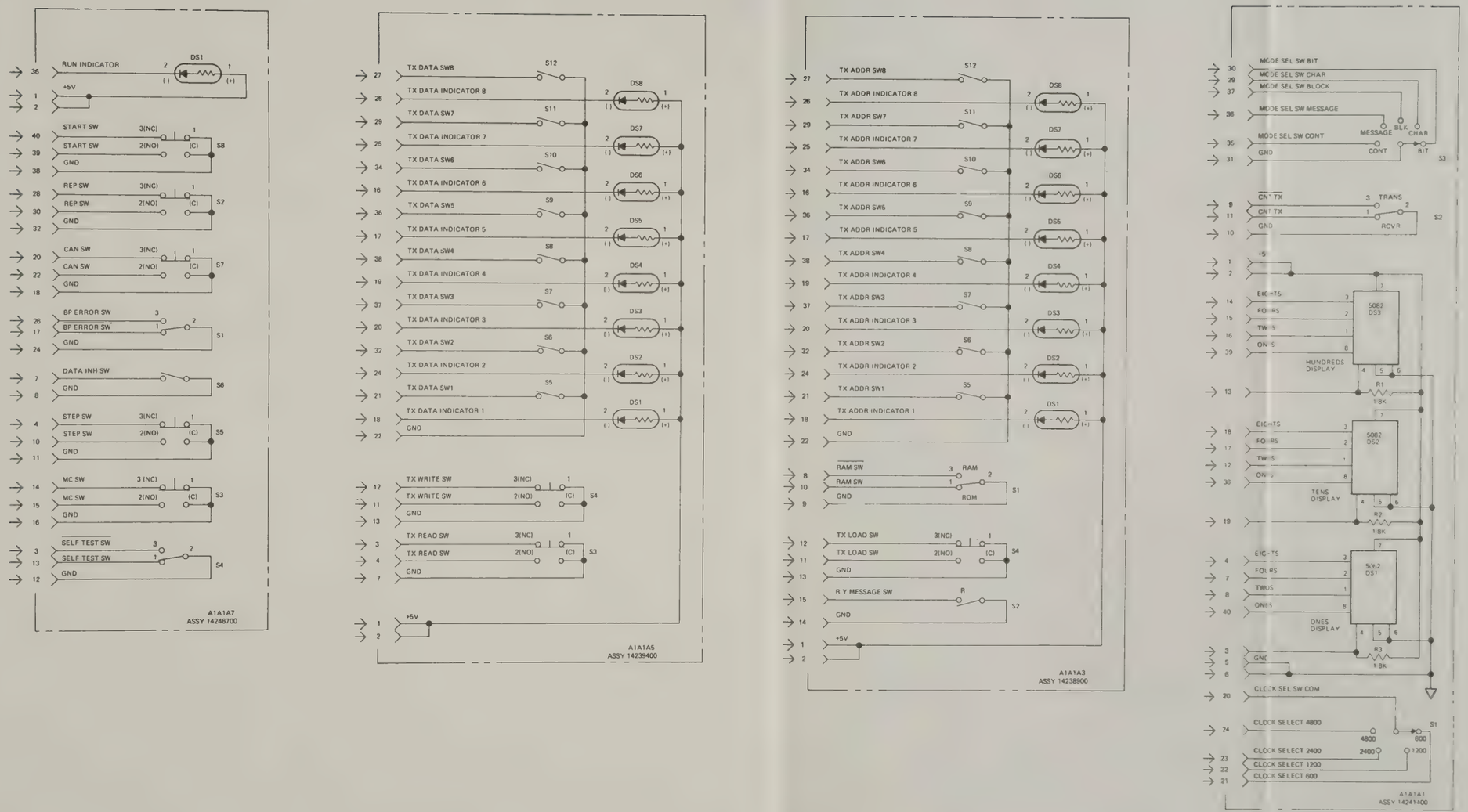
D20005B_/19
(14394700B(01))

Figure 2-6. AIUTE Panel Schematic Diagram (Sheet 1 of 3)



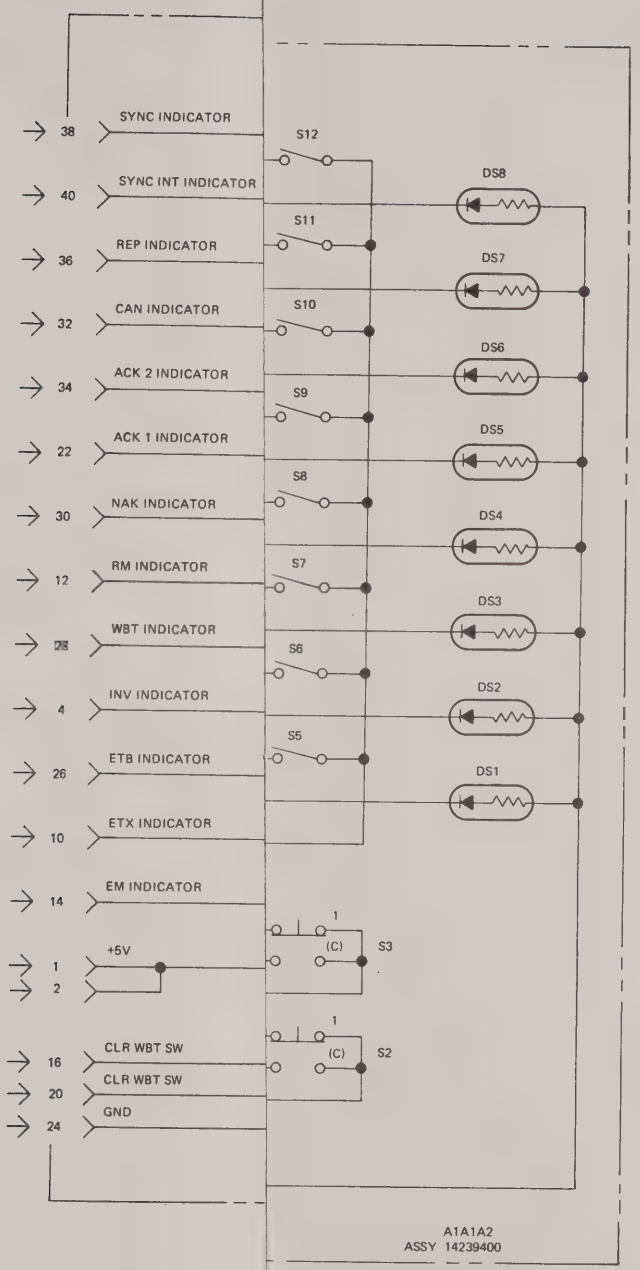
D20005B_/19
(14394700B(02))

l Schematic Diagram
3)



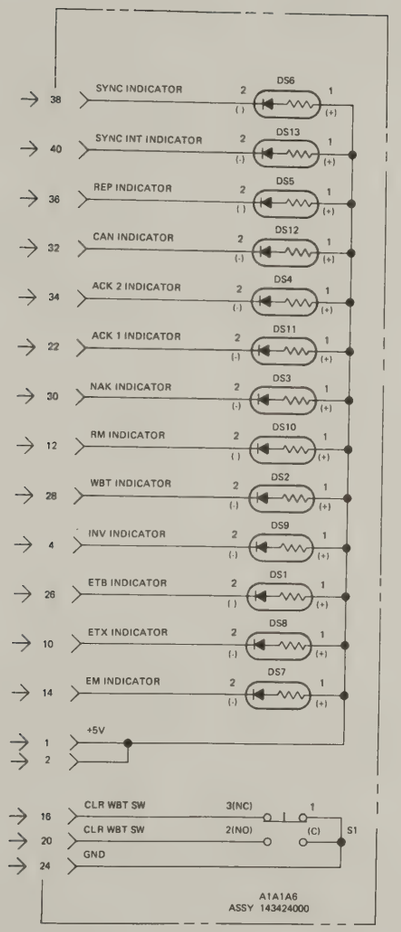
D20005B_/19
(14394700B(02))

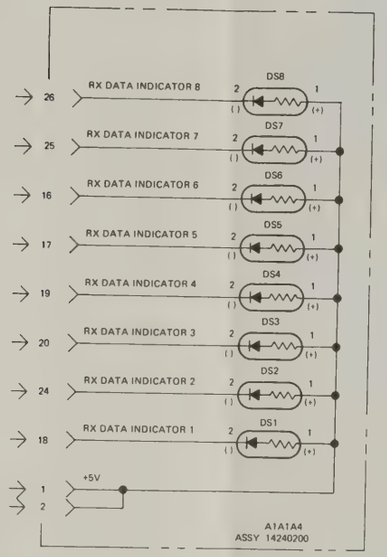
Figure 2-6. AIUTE Panel Schematic Diagram (Sheet 2 of 3)

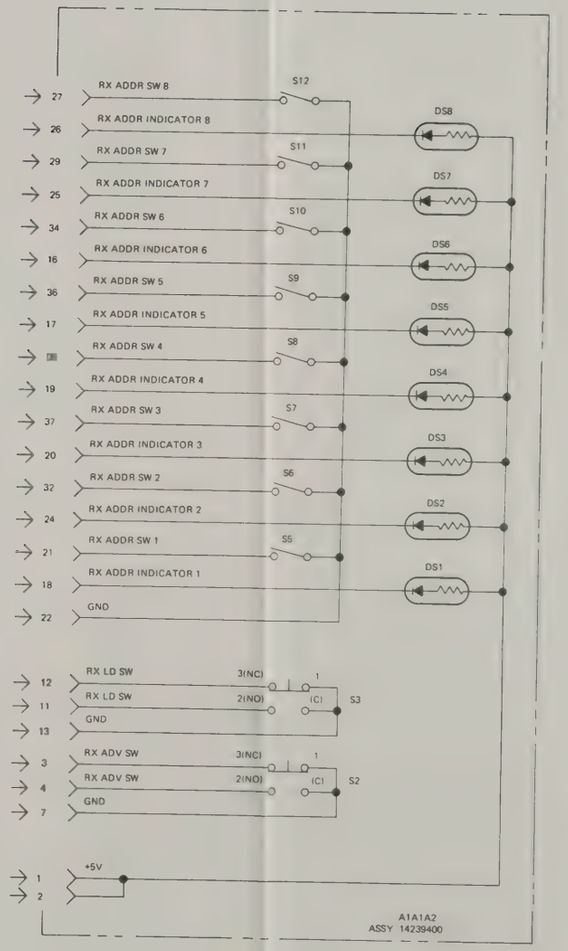


D20005B_/19
(14394700B(03))

nel Schematic Diagram
f 3)







D20005B_/19
(14394700B(03))

Figure 2-6. AIUTE Panel Schematic Diagram (Sheet 3 of 3)

NOTE
1. REFERENCE DRAWING
ASSY. 14242900

D20006B_/19
(14244400B)

terconnection Diagram

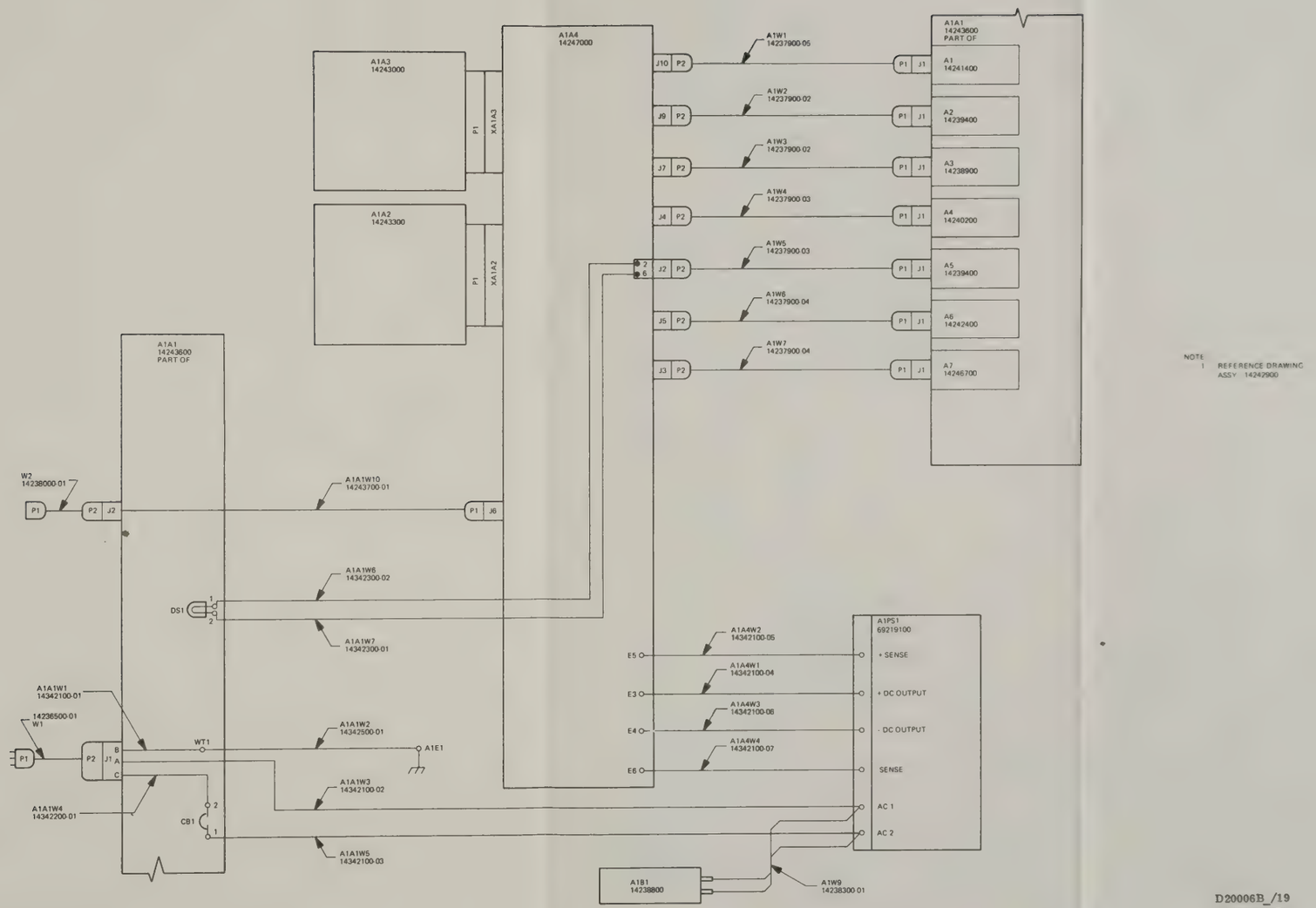


Figure 2-7. AIUTE Interconnection Diagram

CHAPTER 2

SECTION II

SERVICE REQUIREMENTS OF OPERATOR

2-63. SERVICE UPON RECEIPT OF EQUIPMENT.

2-64. INSPECTION. Inspect the AIUTE as follows:

a. Unlatch six cover latches on transit case.

b. Remove cover from main case.

c. Locate hinged panel cover inside case cover.

d. Unlatch panel cover fastener and open panel.

e. Ensure cable assemblies W1 and W2 are stored in cover and remove panel brace.

f. Close panel cover.

g. Loosen captive screws on panel.

h. Grasp panel protector handles, lift hinged panel, and install panel brace.

i. Inspect circuit card assemblies A1A2 and A1A3 to ensure card installation is secure.

j. Remove cable protector panel.

k. Inspect A1W1 through A1W7 to ensure cable installations are secure.

l. Remove any foreign material from chassis enclosure interior.

2-65. COMPLETENESS OF EQUIPMENT. Refer to figure 1-2 to verify completeness of equipment, then proceed as follows:

a. Reinstall cable protector panel and remove panel brace.

b. Close hinged panel and tighten captive screws.

c. Store panel brace in transit case cover.

d. Reinstall transit case cover.

2-66. SERVICE REQUIREMENTS PRIOR TO AND AFTER OPERATION.

2-67. PRIOR TO OPERATION. The AIUTE requires no service prior to operation.

CHAPTER 2

SECTION III

CONTROLS AND INSTRUMENTS

2-68. GENERAL.

2-69. This section describes, locates, illustrates, and furnishes the operators and organizational maintenance personnel sufficient information pertaining to the various controls and instruments provided for operation of the AIUTE.

2-70. AIUTE CONTROLS AND INSTRUMENTS.

2-71. The AIUTE controls and instruments (figure 2-8) consist of some controls and indicators that are common to both the receive and transmit sections, and some that are unique to each section.

2-72. AIUTE COMMON CONTROLS AND INDICATORS. The following controls and indicators are common to the receive and transmit sections:

a. POWER - two-position toggle switch/trip free circuit breaker. When set to ON, ac power is applied to the power supply and blower. When set to OFF, power is removed.

b. POWER - indicator. Lights when dc power from the power supply is applied to the chassis.

c. MODE SELECT - five-position rotary switch:

1. BIT - one bit is received or transmitted each time the STEP switch is pressed. For transmit, the START switch must initially be pressed.

2. CHAR - one character is received or transmitted each time the STEP switch is pressed. For transmit, the START switch must initially be pressed.

3. BLK - one block is received or transmitted. For transmit, the START switch must initially be pressed.

4. MSG - one three-block message is received or transmitted. For transmit, the START switch must initially be pressed.

5. CONT - three block messages are received or transmitted. For transmit, the START switch must initially be pressed.

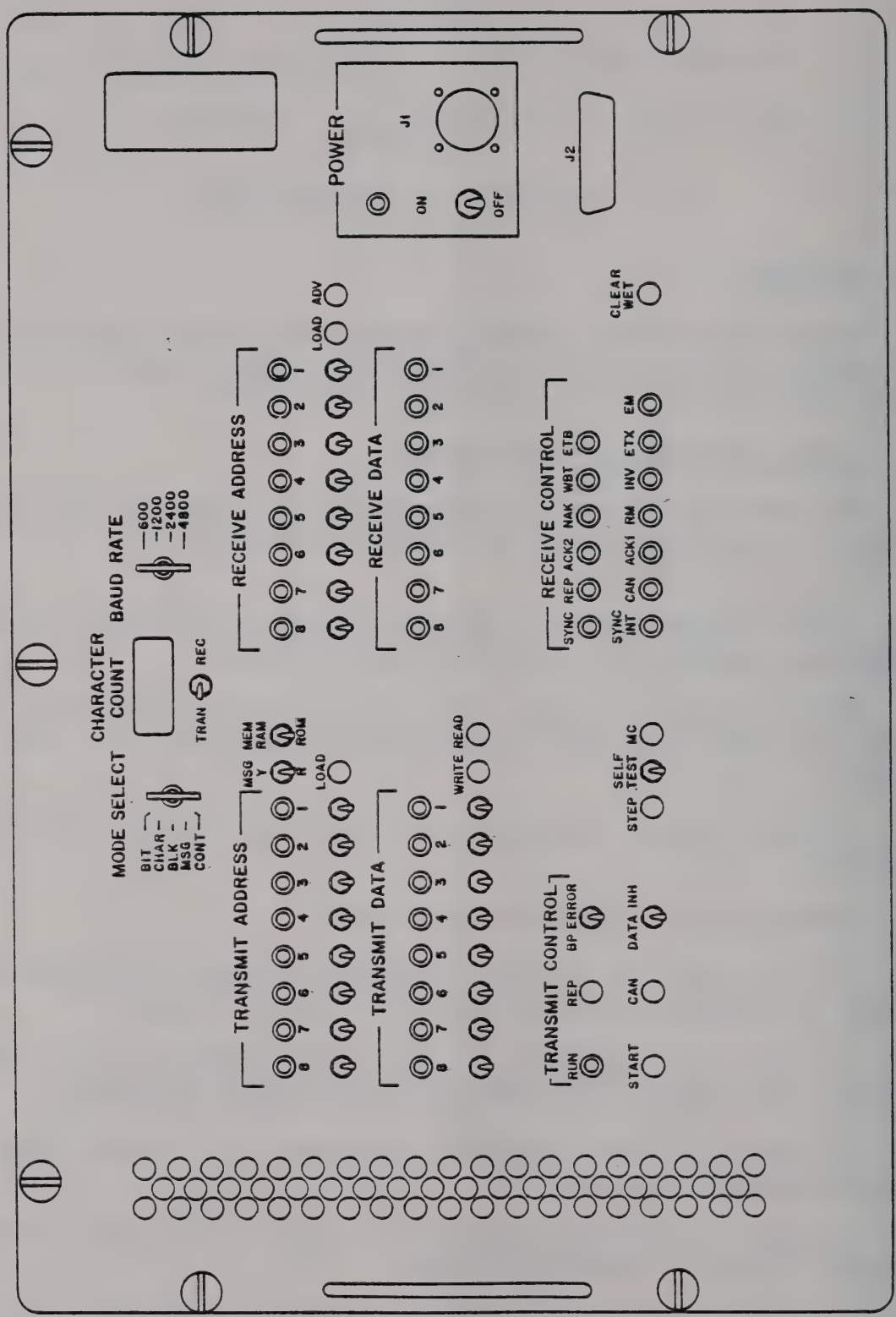


Figure 2-8. AIUTE Controls and Indicators

d. CHARACTER COUNT - three-digit decimal readout display that increments with each character received or transmitted by the AIUTE as determined by the TRAN/REC switch setting.

e. TRAN/REC - two-position toggle switch. When set to TRAN, increments CHARACTER COUNT for each message character read from RAM or ROM. When set to REC, increments CHARACTER COUNT for each message character stored in the RAM.

f. BAUD RATE - four-position rotary switch. The positions 600, 1200, 2400, or 4800 determine the bit transfer baud rate for all AIUTE modes except BIT.

g. STEP - pushbutton switch. Provides operator control of the AIUTE clock for BIT or CHAR mode.

h. SELF TEST - two-position toggle switch. When set to SELF TEST, enables AIUTE receive and transmit back to back operation. When set down, disables self test operation.

i. MC - pushbutton switch. When pressed, the AIUTE is initialized.

2-73. RECEIVER CONTROLS AND INDICATORS. The following controls and indicators are unique to the receiver section:

a. RECEIVE ADDRESS - eight indicators and toggle switches. Indicators display contents of the receiver RAM address register. Two-position toggle switches specify an address for the receiver RAM address register.

b. LOAD - pushbutton switch. When pressed, loads the address specified by the RECEIVE ADDRESS toggle switches.

c. ADV - pushbutton switch. When pressed, advances the current address contained in the receiver RAM address register.

d. RECEIVE DATA - eight indicators that display input data received or data read from the receiver RAM.

e. CLEAR WBT - pushbutton switch. When pressed, clears the WBT control character sequence after a block or message has been received.

f. RECEIVE CONTROL - indicators as follows:

1. SYNC - indicates SYN character received.

2. REP - indicates REP character sequence received.

3. CAN - indicates CAN character sequence received.

4. ACK 2 - indicates ACK 2 character sequence received.

5. ACK 1 - indicates ACK 1 character sequence received.

6. NAK - indicates NAK character sequence received.

7. RM - indicates RM character sequence received.

8. WBT - indicates WBT character sequence received.

9. INV - indicates INV character sequence received.

10. ETB - indicates third frame character received.

11. ETX - indicates third frame character of last message block received.

12. EM - indicates end of medium for magnetic tape message block received.

13. SYNC INT - AIU initiated resynchronization.

2-74. TRANSMITTER CONTROLS AND INDICATORS. The following controls and indicators are unique to the transmit section:

a. TRANSMIT ADDRESS - eight indicators and toggle switches. Indicators display contents of the transmitter memory register. Two-position toggle switches specify an address for the transmitter memory address register.

b. MSG Y/R - toggle switch. Selects DSSCS (Y) or GENSER (R) formatted message contained in the transmitter ROM.

c. MEM RAM/ROM - toggle switch. Selects the transmitter RAM (read/write memory) or ROM (read-only memory).

d. LOAD - pushbutton switch. When pressed, loads the address specified by the TRANSMIT ADDRESS switches into the transmitter memory address register.

e. TRANSMIT DATA - eight indicators and toggle switches. Indicators display data selected from the transmitter RAM, ROM, BP generator, or control character ROM. Toggle switches specify a character for the transmitter RAM write operation.

f. WRITE - pushbutton switch. When pressed, enables a write operation for the transmitter RAM and increments the memory address register.

g. READ - pushbutton switch. When pressed, increments the memory address register by 1 and enables a read operation.

h. TRANSMIT CONTROL - switches as follows:

1. REP - pushbutton switch sends REP control character sequence to AIU.

2. CAN - pushbutton switch sends CAN control character sequence to AIU.

3. BP ERROR - toggle switch forces parity error on BP character sent to AIU.

4. DATA INH - toggle switch sends data inhibit signal to AIU to inhibit AIU transmitter.

5. START - pushbutton switch starts transmit operation.

6. RUN - indicator lights when transmitter is operating.

CHAPTER 2

SECTION IV

OPERATION UNDER SPECIFIC CONDITIONS

2-75. GENERAL.

2-76. The instructions in this section are published for the information and guidance of the personnel responsible for operation of the AIUTE.

2-77. OPERATION UNDER NORMAL CONDITIONS.

2-78. To operate the AIUTE in a test setup configuration, refer to TM-07115A-14, Chapter 3, Section IV, for AIUTE general operating procedures and applicable AIU test procedures using the AIUTE.

SECTION V

OPERATION OF THE EQUIPMENT USED IN CONJUNCTION WITH THE MAJOR ITEM

2-79. DIGITAL ELECTRONIC COUNTER OPERATION.

2-80. To operate the CP-1392/TYC Digital Electronic Counter in conjunction with the AIUTE for troubleshooting, refer to TM-XXXXX-XX, Chapter 2, Section IV.

CHAPTER 3

MAINTENANCE INSTRUCTIONS

SECTION I

INTRODUCTION

3-1. SCOPE.

3-2. This chapter defines maintenance task allocations and contains preventive maintenance information, troubleshooting procedures, and corrective maintenance information for the AIUTE.

3-3. MAINTENANCE TASK ALLOCATIONS.

3-4. This manual contains the intermediate level (echelon 3) maintenance information for the AIUTE. The maintenance task at the intermediate level is limited to the repair of the AIUTE by removal and replacement of failing assemblies. The troubleshooting task is performed by the echelon 3 technician to isolate the trouble to a replaceable assembly. The replacement assembly is determined by the SMR (source maintenance recoverability) code given in the USMC-prepared stock list for the AIUTE.

3-5. MAINTENANCE RECORD AND REPORT FORMS. All maintenance records and reports shall be processed in accordance with the current TM-4700-15/1.

CHAPTER 3

SECTION II

TOOLS AND EQUIPMENT

3-6. TOOLS CARRIED WITH THE EQUIPMENT.

3-7. There are no tools or repair parts carried with the AIUTE.

3-8. SUPPORT EQUIPMENT.

3-9. The CP-1392/TYC Digital Electronic Counter, P/N 14169400-01, is considered support equipment for the AIUTE. Test equipment (handtools, meters, and so forth) carried with the DCT in the shelter can be used for maintenance of the AIUTE.

CHAPTER 3

SECTION III

PREVENTIVE MAINTENANCE

3-10. GENERAL.

3-11. Preventive maintenance for the AIUTE consists of cleaning and inspection. Additionally, when the AIUTE is not in use the transit case cover shall be latched to the main case to ensure a clean environment.

3-12. CLEANING. Cleaning consists of removing any foreign material found during inspection and cleaning the air filter every 6 months as follows:

a. Unlatch transit case cover and remove from main case.

b. Remove panel brace from storage area in case cover.

c. Loosen captive screws on panel.

d. Grasp panel protection handles, raise hinged panel, and install panel brace.

e. Locate air filter mounted on back of panel.

f. Remove air filter mounting screws and air filter.

g. Wash air filter in solution of warm water and mild detergent.

h. Inspect air inlet holes and exhaust outlet.

i. Remove any foreign material.

j. Allow air filter to dry, then reinstall on panel.

k. Remove panel brace.

l. Close hinged panel and tighten captive screws.

m. Store panel brace in case cover.

n. Reinstall case cover and latch.

3-13. INSPECTION. Inspect the AIUTE every 6 months as follows:

a. Unlatch transit case cover and remove from main case.

b. Remove panel brace from storage area in case cover.

c. Inspect cable assemblies W1 and W2 for frayed insulation and connectors for bent, loose, corroded, or broken pins.

d. Inspect panel connectors J1 and J2 for damage.

e. Inspect panel for bent or broken switches or indicators.

f. Loosen captive screws on panel.

g. Grasp panel protection handles, lift hinged panel, and install panel brace.

h. Inspect enclosure for dirt, foreign objects, or corrosion.

i. Inspect wiring for broken, burnt, or frayed wires.

j. Inspect circuit boards A1A2 and A1A3 for cracks or burn spots.

k. Inspect circuit board components for damaged leads.

l. Inspect circuit cards to ensure installation is secure.

m. Inspect cable assemblies A1W1 through A1W7 to ensure installation is secure.

n. Remove panel brace.

o. Close hinged panel and tighten captive screws.

p. Store panel brace in transit case cover.

q. Replace case cover and latch.

NOTE

If corrective maintenance is necessary, refer to Section V of this chapter.

CHAPTER 3

SECTION IV

TROUBLESHOOTING

3-14. AIUTE TROUBLESHOOTING.

3-15. The AIUTE troubleshooting consists of performing test procedures in table 3-1 and the troubleshooting procedures in table 3-2. When a fault occurs during operation of the AIUTE in the test setup, perform the self test procedure in table 3-1 to isolate the fault to the AIUTE. When the fault has been isolated to the AIUTE, or a fault occurs during checkout, refer to the troubleshooting procedures in table 3-2. The troubleshooting procedures provide direction to further isolate the fault to a replaceable assembly. In most cases, the direction consists of checking pins on a switch-indicator assembly to isolate the fault to that assembly or to a pluggable module. Refer to the AIUTE panel schematic diagram (figure 2-6 in Chapter 2, Section I) to identify the switch or indicator pin numbers. For a switch, activate the switch and measure the continuity between pins. For an indicator, measure the continuity between the power and indicator pin in both directions.

3-15. DIGITAL ELECTRONIC COUNTER. The Digital Electronic Counter is useful in troubleshooting the AIUTE. The AIUTE pluggable modules are conformal coated and the pins on the panel interconnect board are not easily accessible; therefore, the use of the Digital Electronic Counter is limited to checking signals at the signal interface cable or the panel interface cables.

Table 3-1. AIUTE Self Test Procedure

ACTION	OBSERVED RESULTS	REMARKS
NOTE: The following steps prepare the AIUTE for self test operation. If any observed result does not occur, go to table 3-2.		
1. Install power cable W1 to J1 on panel.		
2. Plug power cable into convenience outlet on AIU cabinet.		
3. Set SELF TEST up.		
4. Position MODE SELECT to BLK.		
5. Position BAUD RATE to 600.		
6. Set DATA INH down.		
7. Set BP ERROR down.		
8. Set all TRANSMIT ADDRESS and RECEIVE ADDRESS down.		
9. Set all TRANSMIT DATA down.		
10. Set MEM RAM/ROM to RAM.		
11. Set MSG Y/R to R.		
12. Set TRAN/REC to REC.		
13. Set POWER to ON.	POWER indicator lights and fan begins to operate.	
14. Press MC.		
15. Set TRANSMIT ADDRESS 1 up.		

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
16. Press TRANSMIT ADDRESS/ LOAD.	TRANSMIT ADDRESS indicator 1 lights.	
17. Set TRANSMIT DATA 7 and 1 up.		Select character = A.
18. Press TRANSMIT DATA/WRITE.	TRANSMIT DATA indicators 7 and 1 light.	Select character in transmitter RAM.
19. Set MEM RAM/ROM to ROM.		
20. Press MC.	CHARACTER COUNT = 000. RECEIVE CONTROL indicator SYNC lights. TRANSMIT DATA indicators 8, 5, 3, 2 light. RECEIVER DATA indicators 8, 5, 3, 2 light.	 Character synchronization entered. SYN characters being sent to receiver. SYN characters being received from transmitter.
21. Press TRANSMIT CONTROL/ CAN.	RECEIVE CONTROL indicator ACK 2 lights.	Character synchronization complete.
NOTE: The following steps test automatic operation. If any observed result does not occur, go to step 39.		
22. Press TRANSMIT CONTROL/ START.	RUN lights, then goes off after: CHARACTER COUNT = 084. RECEIVE CONTROL indicator REP flashing. RECEIVE CONTROL indicator WBT flashing. RECEIVE CONTROL indicator ETB lights.	
23. Press CLEAR WBT.	RECEIVE CONTROL indicators ACK 1 and SYNC light.	First block transfer test complete.

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
24. Press TRANSMIT CONTROL/ START.	RUN lights, then goes off after: CHARACTER COUNT = 168. RECEIVE CONTROL indicator REP flashing. RECEIVE CONTROL indicator WBT flashing. RECEIVE CONTROL indicator ETB lights.	
25. Press CLEAR WBT.	RECEIVE CONTROL indicators ACK 2 and SYNC light.	Second block transfer test complete.
26. Press TRANSMIT CONTROL/ START.	RUN lights, then goes off after: CHARACTER COUNT = 252. RECEIVE CONTROL indicator REP flashing. RECEIVE CONTROL indicator WBT flashing. RECEIVE CONTROL indicator ETX lights.	
27. Press CLEAR WBT.	RECEIVE CONTROL indicators ACK 1 and SYNC light.	Third block transfer test complete.
28. Set MODE SELECT to MSG.		
29. Press MC.		
30. Press START.	RECEIVE CONTROL indicator RM lights.	
31. Press MC and then press TRANSMIT CONTROL/CAN.	RECEIVE CONTROL indicator ACK 2 lights.	

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
32. Press TRANSMIT CONTROL/ START.	RUN indicator lights, then goes off after: CHARACTER COUNT = 252. RECEIVE CONTROL indicator ETX lights.	Message transfer test complete.
33. Set MODE SELECT to CONT.		
34. Press MC and then press TRANSMIT CONTROL/CAN.	RECEIVE CONTROL indicator ACK 2 lights.	
35. Press TRANSMIT CONTROL/ START.	RUN indicator lights and RECEIVE CONTROL indicators. ACK 1 and ACK 2 light alternately each time SYNC indicator flashes.	
36. Set TRANSMIT CONTROL/ BP ERROR up.	RUN indicator lights, then goes off after: RECEIVE CONTROL indicator NACK lights. RECEIVE CONTROL indicator SYNC lights. RECEIVE CONTROL indicator ETB or ETX lights.	
37. Set BP ERROR down.		Forced block parity error test complete.
38. Press MC and then press TRANSMIT CONTROL/CAN.	RECEIVE CONTROL indicator ACK 2 lights.	

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
NOTE: The following steps test clock step operation character by character. If observed result for any character does not occur, go to table 3-2.		
39. Set MODE SELECT to CHAR.		
40. Press TRANSMIT CONTROL/ START.		
41. Press STEP.	TRANSMIT CONTROL/RUN indicator lights.	Transmits SYN character and selects SOH character
42. Press STEP,	TRANSMIT ADDRESS indicator 1 lights.	Transmits SOH character and selects A (select) character.
43. Press STEP.	TRANSMIT ADDRESS indicator 2 lights. RECEIVE ADDRESS indicator 1 lights. CHARACTER COUNT = 001. RECEIVE CONTROL indicator SYNC off.	Transmits A (select) character and selects R character. Receiver writes SOH character in RAM and increments address. Receiver increments character count.
44. Press STEP repeatedly until CHARACTER COUNT = 083.	CHARACTER COUNT = 083. RECEIVE DATA indicators 5, 3, 2, 1 light. RECEIVE CONTROL indicator ETB lights.	Address and data bits are defined in table 2-1. 83rd character should be ETB character.
45. Press STEP.	CHARACTER COUNT = 084. TRANSMIT CONTROL/RUN indicator goes off.	Block parity character received and written in the receiver RAM.

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
46. Press STEP four times.	RECEIVE CONTROL indicator ACK 1 lights. RECEIVE CONTROL indicator SYNC lights.	First block transfer test complete.
47. Press TRANSMIT CONTROL/ START.		
48. Press STEP.	TRANSMIT CONTROL/RUN indicator lights. TRANSMIT ADDRESS indicators 7, 5, 3 light.	Transmits SYN character and selects STX character.
49. Press STEP.	TRANSMIT ADDRESS indicators 7, 5, 3, 1 light.	Transmits STX character and selects DEL character.
50. Press STEP.	TRANSMIT ADDRESS indicators 7, 5, 3, 2 light. RECEIVER ADDRESS indicators 7, 5, 3, 1 light. CHARACTER COUNT = 085.	Transmits DEL character and selects A (text) character. Receiver writes DEL character in RAM and increments address. Receiver increments character count.
51. Press STEP repeatedly until CHARACTER COUNT = 167.	CHARACTER COUNT = 167. RECEIVE DATA indicators 5, 3, 2, 1 light. RECEIVE CONTROL indicator ETB lights.	Address and data bits are defined in table 2-1. 167th character should be ETB.
52. Press STEP.	CHARACTER COUNT = 168. TRANSMIT CONTROL/RUN indicator goes off.	Block parity character received and written in the receiver RAM.
53. Press STEP four times.	RECEIVE CONTROL indicator ACK 2 lights. RECEIVE CONTROL indicator SYNC lights.	Second block transfer test complete.

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
54. Press START.		
55. Press STEP.	TRANSMIT CONTROL/RUN indicator lights. TRANSMIT ADDRESS indicators 8,6,4 light.	Transmits SYN character and selects STX character.
56. Press STEP.	TRANSMIT ADDRESS indicators 8,6,4,1 light.	Transmits STX character and selects DEL character.
57. Press STEP.	TRANSMIT ADDRESS indicators 8,6,4,2 light. RECEIVE ADDRESS indicators 8,6,4,1 light. CHARACTER COUNT = 169.	Transmits DEL character and selects * character. Receiver written STX character in RAM and increments address. Receiver increments character count.
58. Press STEP repeatedly until CHARACTER COUNT = 251.	CHARACTER COUNT = 251. RECEIVE DATA indicators 2, 1 light. RECEIVE CONTROL indicator ETX lights.	Address and data bits are defined in table 2-1. 251st character should be ETX.
59. Press STEP.	CHARACTER COUNT = 252.	Block parity character received and written in the receiver RAM.
60. Press MC and then press TRANSMIT CONTROL/CAN.	TRANSMIT CONTROL/RUN indicator goes off. RECEIVE CONTROL indicator ACK 2 lights.	Third block transfer test complete.

Table 3-1. AIUTE Self Test Procedure (Cont.)

ACTION	OBSERVED RESULTS	REMARKS
NOTE: The following steps test clock step operation bit by bit. If the observed result for any bit step transfer does not occur, go to table 3-2. To test a character in the first block, go to step 39 and step the character count up to the desired character, then perform the procedure below. To test a character in second or third block, set the MODE SELECT switch to BLK, go to step 20 and start the block transfer up to the desired block, set the MODE SELECT switch to CHAR, and go to step 48 or 55. Then, step the character count up to the desired character and perform the procedure below.		
61. Position MODE SELECT switch to BIT.		
62. Press STEP switch.		
63. Press STEP switch eight times for each character.	ADDRESS indicators display address. DATA indicators display data.	Address and data bits are defined in table 2-1.

Table 3-2. AIUTE Troubleshooting

SYMPTOM	PROBABLE CAUSE	REMEDY
1. POWER indicator off, blower fan not operating.	Power source.	Check cable 1W1 at AIU outlet. Check shelter power distribution box.
	Power switch A1A1CB1,	Set to ON. Check switch and replace it if necessary.
2. Power indicator off, blower fan operating.	Power indicator A1A1DS1.	Check indicator wiring. Replace indicator if necessary.
	Power supply A1PS1.	Check power supply output. Replace power supply if necessary.
3. Power indicator lights, blower fan not operating.	Cable A1W9. Blower A1B1.	Plug in to blower fan. Check blower fan assembly and replace if necessary. **CAUTION** To prevent damage to the equipment, set POWER to OFF before unplugging cable in the following steps.
4. RECEIVE ADDRESS indicators off in test.	Pluggable module A1A2. Switch-indicator assembly A1A1A2.	Unplug A1W2P1 and check A1A1A2J1 pins for RECEIVE ADDRESS switch and indicator and RECEIVE ADDRESS LOAD or ADV switch.
5. TRANSMIT ADDRESS indicators off in test.	Pluggable module A1A3. Switch-indicator assembly A1A1A3.	Unplug A1W3P1 and check A1A1A3J1 pins for TRANSMIT ADDRESS switch and indicator and TRANSMIT ADDRESS LOAD switch.
6. RECEIVE DATA indicators off in test.	Pluggable module A1A2. Switch-indicator assembly A1A1A4.	Unplug A1W4P1 and check A1A1A4J1 pins for RECEIVE DATA indicator.

Table 3-2. AIUTE Troubleshooting (Cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
7. TRANSMIT DATA indicators off in test.	Pluggable module A1A3, Switch-indicator assembly A1A1A5.	Unplug A1W5P1 and check A1A1A5J1 pins for TRANSMIT DATA switch and indicator and TRANSMIT WRITE or READ switch.
8. RECEIVE CONTROL indicator off in test.	Pluggable module A1A2, Switch-indicator assembly A1A1A6.	Unplug A1W6P1 and check A1A1A6J1 pins for indicators.
9. No ACK after CLR WBT in test.	Pluggable module A1A2, Switch-indicator assembly A1A1A6.	Unplug A1W6P1 and check A1A1A6J1 pins for CLEAR WBT switch.
10. No RECEIVE CONTROL indication after TRANSMIT CONTROL/START, REP, CAN, or BP ERROR switch action in test.	Pluggable module A1A3, Switch-indicator assembly A1A1A7.	Unplug A1W7P1 and check A1A1A7J1 pins for TRANSMIT CONTROL switch.
11. No TRANSMIT CONTROL/ RUN indication in test.	Pluggable module A1A3, Switch-indicator assembly A1A1A7.	Unplug A1W7P1 and check A1A1A7J1 pins for RUN indicator.
12. No SYNC, TRANSMIT DATA, and RECEIVE DATA indication after MC switch action in test.	Pluggable module A1A3, Switch-indicator assembly A1A1A7.	Unplug A1W7P1 and check A1A1A7J1 pins for MC switch.
13. No RECEIVE ADDRESS, RECEIVE DATA, or RECEIVE CONTROL indication after STEP switch action in test.	Pluggable module A1A3, Switch-indicator assembly A1A1A7.	Unplug A1W7P1 and check A1A1A7J1 pins for STEP switch.
14. No TRANSMIT DATA indication with SELF TEST switch set and MC switch action.	Pluggable module A1A3, Switch-indicator assembly A1A1A7.	Unplug A1W7P1 and check A1A1A7J1 pins for SELF TEST switch.

Table 3-2. AIUTE Troubleshooting (Cont.)

SYMPTOM	PROBABLE CAUSE	REMEDY
15. No RUN indication with MODE SELECT set to BIT CHAR after STEP switch action in test.	Pluggable module A1A3. Switch-indicator assembly A1A1A1.	Unplug A1W1 and check A1A1A1J1 pins for MODE SELECT switch.
16. REP only indication with MODE SELECT set to BLK or MSG after START switch action in test.	Pluggable module A1A2. Switch-indicator assembly A1A1A1.	Unplug A1W1 and check A1A1A1J1 pins for MODE SELECT switch.
17. No RUN indication with MODE SELECT set to CONT after START switch action in test.	Pluggable module A1A3. Switch-indicator assembly A1A1A1.	Unplug A1W1 and check A1A1A1J1 pins for MODE SELECT switch.
18. CHARACTER COUNT does not increment properly in test.	Pluggable module A1A3. Switch-indicator assembly A1A1A1.	**CAUTION** Use care in performing the following procedure to prevent damage to equipment. With AIUTE in SELF TEST for character mode, proceed as follows: 1. Locate circuit paths on A1A1A1 to character counter. 2. Step character and check A1A1A1DS1 for proper count code.

CHAPTER 3

SECTION V

CORRECTIVE MAINTENANCE

3-16. INTRODUCTION.

3-17. This section contains the procedure for removing and replacing the field-replaceable subassemblies and components in the AIUTE.

3-18. REMOVAL AND REPLACEMENT.

3-19. The following removal and replacement procedures provide corrective maintenance to support the troubleshooting procedures.

CAUTION

To prevent damage to equipment, remove ac power from the AIUTE and the subsystem under test before performing replacement procedures.

3-20. PLUGGABLE MODULE REPLACEMENT. To remove and replace pluggable module A1A2 or A1A3, proceed as follows:

a. Position POWER toggle switch to OFF and unplug power cable from convenience outlet.

b. Loosen captive screws on AIUTE panel.

c. Remove panel brace from case cover.

d. Grasp panel protection handles, raise hinged panel, and install panel brace.

e. Loosen module holddown bar screws sufficiently to remove pressure on edges of module.

f. Locate frame at top of module and extractor cutout in center of frame.

g. Insert screwdriver through cutout.

h. Separate module connector from receptacle by carefully forcing screwdriver against block on bracket under frame (located on edge opposite module connector).

i. Remove module holddown bars.

j. Remove module.

CAUTION

Align module properly to prevent bent or broken connector pins when replacing module.

k. Align module connector with receptacle and push in slightly to engage connector with receptacle.

l. Reinstall module holddown bars sufficiently to seat on edges of module.

m. Apply force on screwdriver against bracket block to fully mate module connector with receptacle.

n. Tighten module holddown bar screws.

o. Remove panel brace.

p. Grasp panel protection handles and lower hinged panel.

q. Tighten captive screws on panel.

r. Store panel brace in case cover.

3-21. SWITCH-INDICATOR ASSEMBLY REPLACEMENT. To remove and replace one of the switch-indicator assemblies, A1A1A1 through A1A1A7, proceed as follows:

a. Position POWER toggle switch to OFF and unplug power cable from convenience outlet.

b. Loosen captive screws on panel.

c. Remove panel brace from case cover.

d. Grasp panel protection handles, raise hinged panel, and install panel brace.

e. Locate switch-indicator assembly components on front of panel.

f. Remove nut and washer from each component on switch-indicator assembly.

g. Remove flat cable protector panel.

h. Locate switch-indicator assembly at rear of panel.

i. Unplug cable connector P1 from connector J1 on switch indicator assembly.

j. Locate and remove four mounting screws on switch-indicator assembly.

k. Remove assembly and mounting hardware (see figure 3-1).

l. Position replacement switch-indicator assembly on rear of panel for installation.

m. Install and tighten five mounting screws.

n. Locate components on front of panel.

o. Install and tighten component mounting hardware.

p. Plug cable connector P1 into connector J1 on replaced switch-indicator assembly.

q. Reinstall flat cable protector panel.

r. Remove panel brace.

s. Grasp panel protection handles and lower panel.

t. Tighten captive screws on panel.

u. Store panel brace in case cover.

3-22. POWER INDICATOR. To remove and replace power indicator A1A1DS1, proceed as follows:

a. Position POWER toggle switch to OFF and unplug power cable from convenience outlet.

b. Loosen captive screws on panel.

c. Remove panel brace from case cover.

d. Grasp panel protection handles, raise hinged panel, and install panel brace.

e. Locate component on back of panel.

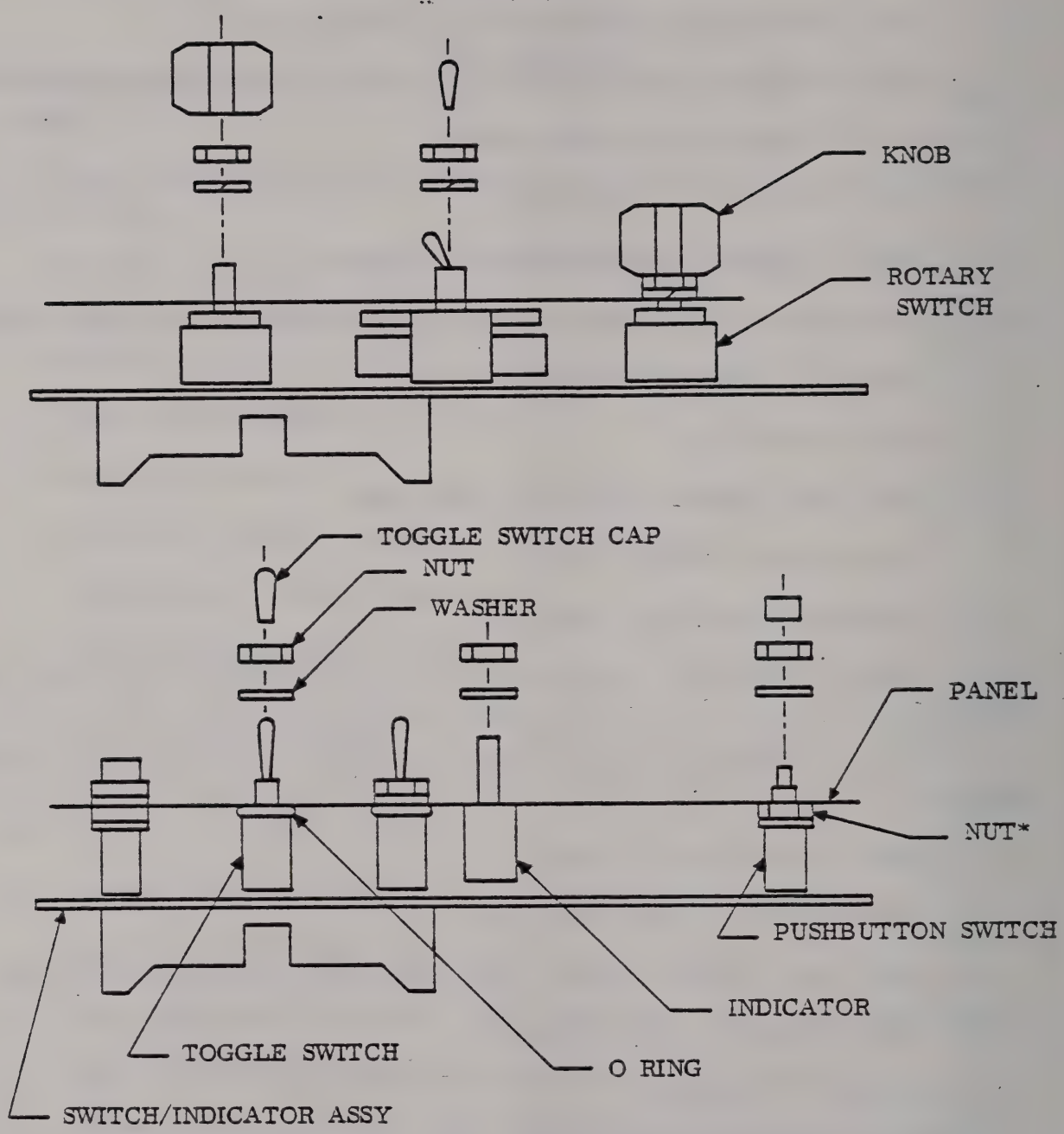
f. Tag wires to component.

g. Remove slip-off terminals for A1A1DS1.

h. Locate component on front of panel and remove mounting hardware and component.

i. Position replacement component in panel cutout.

j. At front of panel, install component hardware.



*ALL PUSHBUTTON SWITCHES MUST HAVE A NUT BETWEEN THE SWITCH BODY AND PANEL.

Figure 3-1. Switch-Indicator Assembly Replacement

k. At rear of panel, reinstall slip-off terminals for A1A1DS1.

l. Remove tags.

m. Remove panel brace.

n. Grasp panel protection handles and lower hinged panel.

o. Tighten captive screws on panel.

p. Store panel brace in case cover.

3-23. BLOWER ASSEMBLY REPLACEMENT. To remove and replace the blower assembly A1B1, proceed as follows:

a. Position POWER toggle switch to OFF and unplug power cable from convenience outlet.

b. Unplug power and signal cable assemblies at panel connectors A1J1 and A1J2.

c. Loosen captive screws on panel.

d. Remove panel brace from case cover.

e. Grasp panel protection handles, raise hinged panel, and install panel brace.

f. On wired I/O assembly chassis flange, remove eight screws.

g. Lift wired I/O assembly chassis to separate it from transit case.

h. Locate cable A1W9 and unplug cable connector from blower assembly.

i. Locate blower assembly mounting hardware.

j. Remove mounting hardware and blower assembly.

k. Position replacement blower assembly over chassis mounting holes.

l. Reinstall mounting hardware.

m. Locate cable A1W9 and plug cable connector into blower assembly.

n. Place chassis in transit case and secure with eight screws.

o. Remove panel brace.

p. Grasp panel protection handles and lower panel.

q. Tighten captive screws on panel.

r. Store panel brace in case cover.

3-24. POWER SUPPLY REPLACEMENT. To remove and replace power supply A1PS1, proceed as follows:

a. Position POWER toggle switch to OFF and unplug power cable at convenience outlet.

b. Unplug power and signal cable assemblies at panel connectors A1J1 and A1J2.

c. Loosen captive screws on panel.

d. Remove panel brace from case cover.

e. Grasp panel protection handles, raise hinged panel, and install panel brace.

f. On wired I/O assembly chassis mounting flange, remove eight screws.

g. Lift wired I/O assembly chassis to separate it from transit case.

h. Refer to replacement procedure for pluggable modules and remove A1A2 and A1A3. After removal of pluggable modules, proceed to next step.

i. Locate power supply terminal strip through bracket cutout.

j. Tag and disconnect wires to terminal strip.

k. Remove power supply mounting hardware.

l. Maneuver power supply to remove it through bracket cutout.

m. Apply heat transfer compound and position replacement power supply over chassis mounting holes.

n. Reinstall power supply mounting hardware.

o. Attach tagged wires to terminal strip on power supply and remove tags.

p. Refer to replacement procedure for pluggable modules and replace A1A2 and A1A3 modules.

q. Place wired I/O chassis in transit case and secure with eight screws.

r. Remove panel brace.

s. Grasp panel protection handles and lower panel.

t. Tighten captive screws.

u. Store panel brace in case cover.